Chip-Package Co-Design of Integrated Mixed Signal Systems

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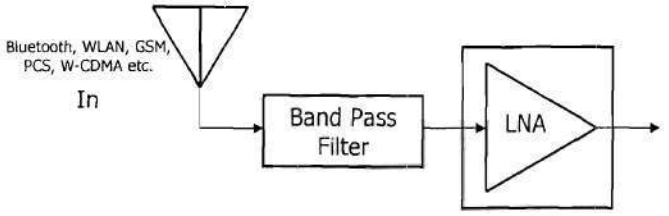
Outline

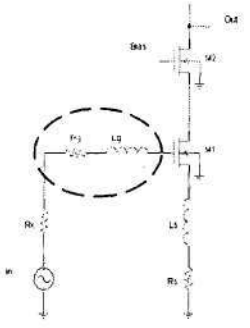
- Introduction
- Inductively degenerated CMOS LNA and inductor design optimization
- Multiple embedded passives and effect of ground return layout on system performance
- Modeling of coupling between multiple passives embedded in the package
- Conclusion

Standard RF Front-End



- Low Noise Figure (NF)
- Input impedance match
- Reasonable gain
- Low power consumption

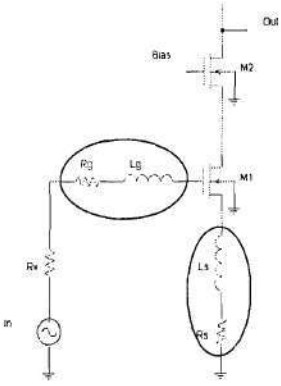
Previous Work



Author	Year	Frequency (GHz)	NF (dB)	Gain (dB)
Karanicolas et al.	1996	0.9	2.2	15.6
Shaeffer et al.	1997	1.5	3.5	22
Hayashi et al.	1998	0.9	1.8	14.8
Huang et al	1998	0.9	1.85	16.2
Floyd et al	1999	0.9	1.2	9.4
Gramegna et al.	2000	0.9	1.8	8.2
Abou-Allem et al.	2001	1.9	1.8	15
Gramegna et al.	2001	0.9	0.85	15

Uses **external discrete components** (inductors) to complete the circuit

Effect of Finite Inductor Q



- On-chip inductors for ordinary CMOS processes have low Q (5-15)
- Ls very small (<2nH), can be easily implemented inside the chip
- Lg can range from 5-35 nH. Impossible to implement this on-chip and still meet performance specs

Noise Figure Derivation

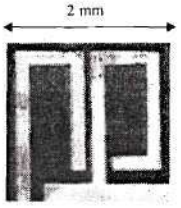
$$NF = \frac{(SNR)_{in}}{(SNR)_{out}}$$

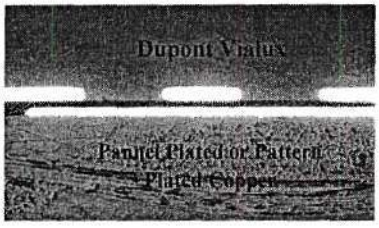
$$NF = 1 + \frac{R_g}{R_x} + \frac{R_{gate}}{R_x} + \frac{R_s}{R_x} + \frac{\beta_1 \omega_0^2 C_{GS}^2 (\omega_0^2 L_T^2 + (R_x + R_g + R_{gate} + R_s)^2)}{R_x g_{dn}}$$

$$+ \frac{2c\omega_0^2 C_{GS}^2 (R_x + R_g + R_{gate} + R_{ch} + R_s)(R_x + R_g + R_{gate} + R_s)\sqrt{\gamma_1 \beta_1}}{g_m R_x}$$

$$+ \frac{\omega_0^2 C_{GS}^2 (R_x + R_g + R_{gate} + R_{ch} + R_s)^2 \gamma_1 g_{dn}}{g_m^2 R_x}$$

High Q Embedded Passives in Organic Substrates

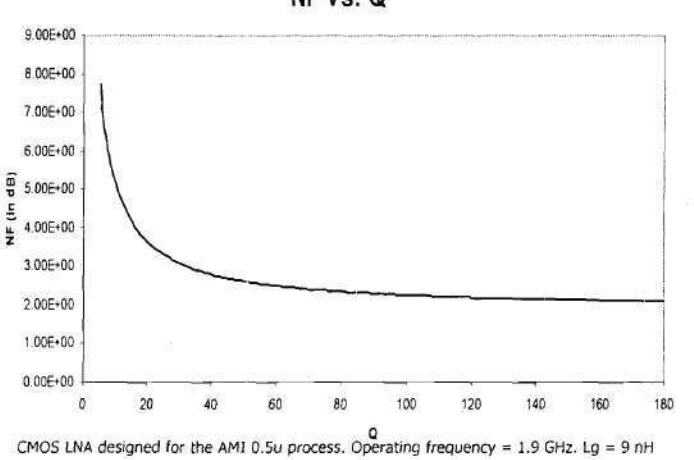




Type	Max Q	Inductance	SRF	Area (mm^2)
CPW Circular Large	160 @ 1.8 GHz	16nH	>3.6GHz	25
CPW Circular Small	170 @ 2.2 GHz	9nH	>4.5GHz	28
1 turn microstrip	170 @ 2.4 GHz	1.6nH	>5GHz	3.5
2 turn microstrip	110 @ 2 GHz	5nH	> 5GHz	4.1
3 turn microstrip	100 @ 1.2 GHz	12nH	>3GHz	3
1.75 loop microstrip	110 @ 2.1 GHz	7.7nH	>4.3GHz	4
2 loop CPW	110 @ 1.8 GHz	9nH	>3.6GHz	9
2by2 loop CPW	80 @ 1.8 GHz	14nH	>3.6GHz	9
1.75 loop CPW	150 @ 2.2 GHz	5 nH	>4.5 GHz	9

Ref: Dalmia S. et al., "Design and optimization of high Q RF passives on SOP based organic substrates", *Proceedings of the Electronic Components and Technology Conference (ECTC)*, 2002.

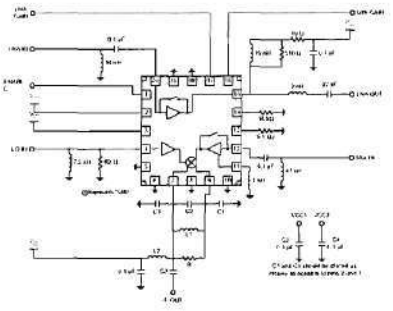
Variation in NF with Gate Inductor Q



CMOS LNA designed for the AMI 0.5u process. Operating frequency = 1.9 GHz. Lg = 9 nH

Multiple Embedded Passives

Application Schematic - US PCS

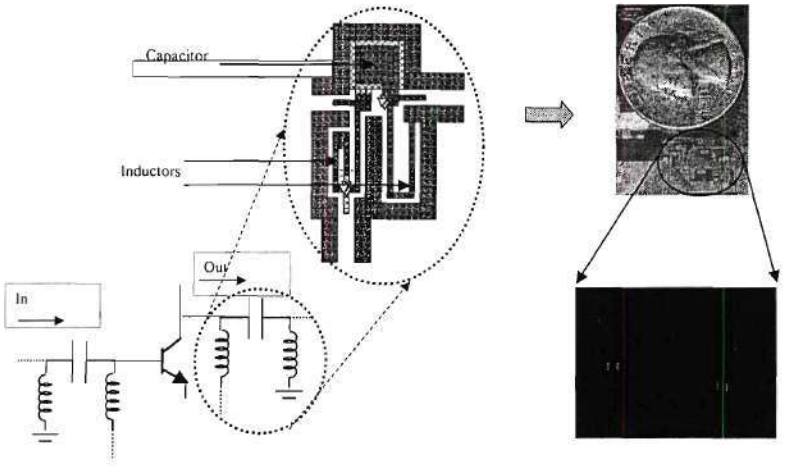


RF2460™ PCS CDMA Low Noise Amplifier/Mixer 1500MHz to 2200 MHz Downconverter from RF Micro Devices (RFMD™)

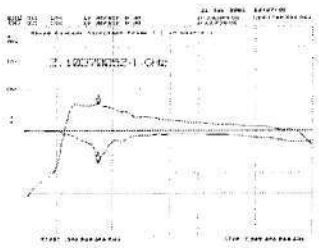
- Complete integration at the package level requires multiple embedded passives in the package substrate
- *Coupling between embedded passives result in feedback and instability*

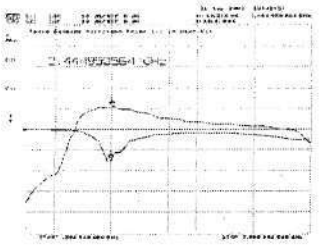
Efficient and accurate modeling of coupling between embedded passives necessary

Test Vehicle: LNAs with Multiple Embedded Passives



Measurements

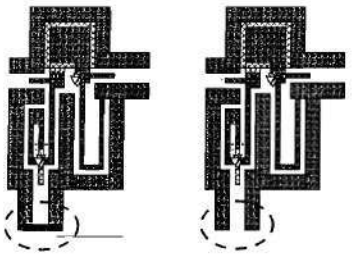




Performance Summary

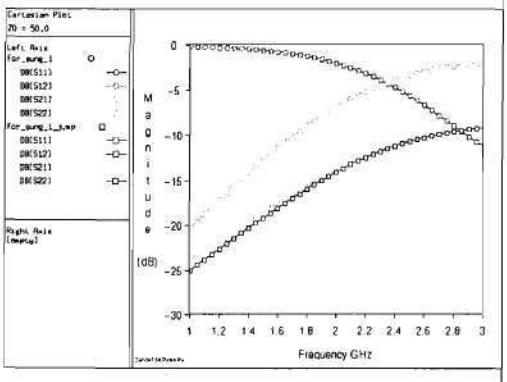
	Circuit 1	Circuit 2
Frequency	2.1 Ghz	2.44 GHz
Gain (S_{21})	12.74 dB	10.5 dB
Input Match (S_{11})	-14.01 dB	-13.772 dB
NF (simulated)	2.5 dB	2.8 dB
P_{-1}	-8.9 dB	-9.2 dB
Supply Voltage	3.5 V	3.5 V
Supply Current	7 mA	7 mA

Effect of Reference Ground Layout in System Performance

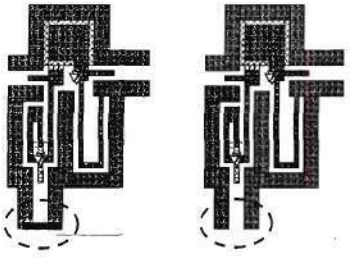


Topology 1 Topology 2

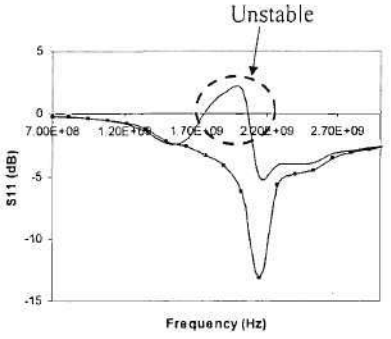
Two reference ground layout topologies for the input pi. Topology 1 uses a jumper to change the return current path.



Effect of Reference Ground Layout in System Performance

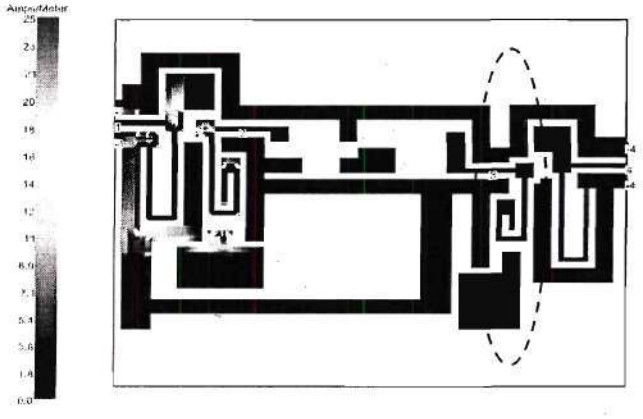


Topology 1 Topology 2

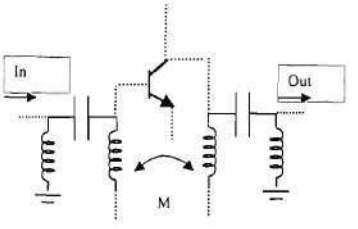


Two reference ground layout topologies for the input pi. Topology 1 uses a jumper to change the return current path.

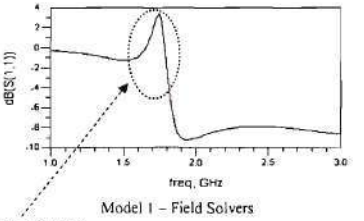
Modeling 1 – Field Solvers



Modeling 1 – Field Solvers (ctd.)

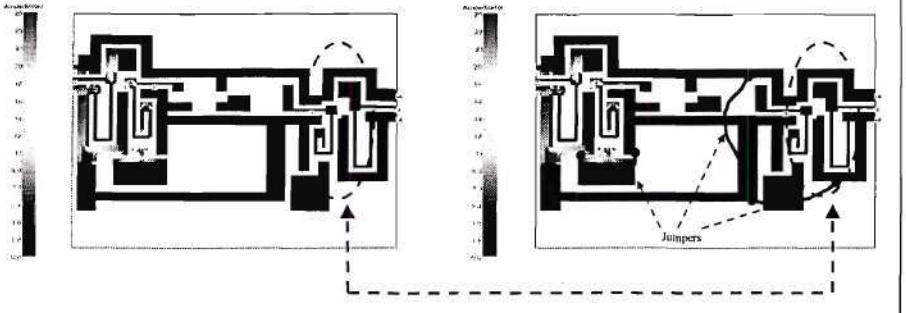


Modeled S11 showing instability

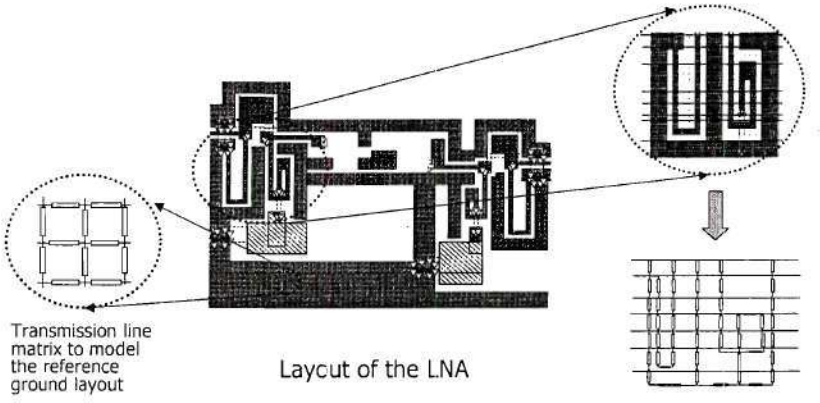


S11>0 at 1.8 GHz

Modeling 1 – Field Solvers (ctd.)



Modeling 2 – Segmentation and Coupled Line Theory



Transmission line matrix to model the reference ground layout

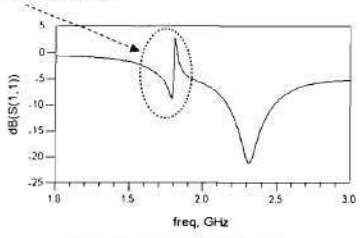
Laycut of the LNA

Segmentation and coupled line modeling of signal carrying traces and passives networks

Modeling 2 – Segmentation and Coupled Line Theory (ctd.)

Modeled S11 showing instability

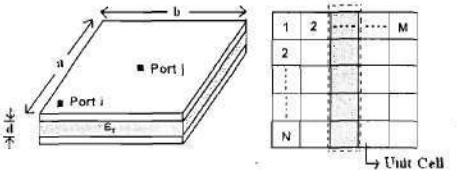
S11>0 at 1.8 GHz



Model 2 – Coupled Line Theory

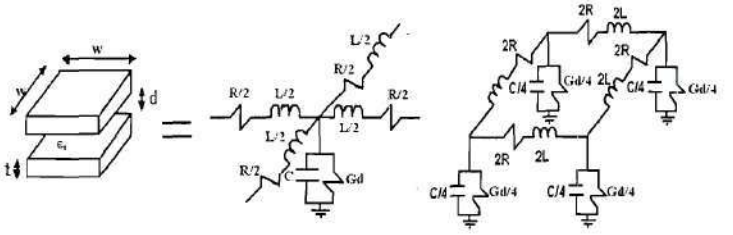
Reduction in computational simulation time by **10x**, when compared to Modeling Approach 1 using SONNET

Future Work: Transmission Matrix Model



$$C = \varepsilon \frac{a^2}{d} \qquad L = u_o d$$

$$R_{dc} = \frac{2}{\sigma_c t} \qquad R_{ac} = 2\sqrt{\frac{\pi f \mu_c}{\sigma_c}} \qquad R_d = \frac{1}{\omega C \tan\delta}$$



Ref. Joong-Ho Kim and Madhavan Swaminathan, "Modeling of Irregular Shaped Power Distribution Planes Using Transmission Matrix Method", *IEEE Trans. On Advanced Packaging*, Vol 24, No. 23, Aug 2001.

Conclusions

- Inductor design optimization for chip-package co-design of integrated CMOS LNAs have been proposed
- The effect of coupling between multiple passives and return current routing on system performance has been studied, and experimentally verified through the design of low noise amplifiers operating at 2.1 and 2.44 GHz respectively
- A design and simulation methodology to integrate system level full-wave solvers into the design process for active devices with multiple embedded passives has been proposed. A computationally efficient circuit based modeling technique using coupled-line theory has also been developed

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- National Science Foundation (NSF) and Semiconductor Research Corporation (SRC)

Design and Implementation of RF Subsystems with Multiple Embedded Passives in Multi-Layer Organic Substrates

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Abstract — **Recent developments in the design of high-Q passives embedded in low cost IC packages have made single-package integration of RF front-ends feasible. This paper analyses the effect of ground return on the performance of active circuits, while using multiple embedded devices in the package. The return-current path layout has been modeled using both electromagnetic field solvers as well as a circuit-based modeling methodology based on coupled line theory. Low noise amplifiers (LNAs) using discrete and embedded components have been designed and fabricated as test vehicles, and the modeled results have been verified with measurements.**

I. Introduction

The unavailability of high-Q passives on-chip has been a major roadblock in the design of integrated single-chip RF devices. In recent years, several publications have reported the design of high-Q passives embedded in organic packaging material ([1]). As any circuit has to be packaged for thermal and mechanical protection, this System-on-Package (SOP) approach provides an opportunity to achieve complete integration without any extra cost. However, higher levels of system integration require multiple passives to be embedded in the package. For example, the phase noise of a voltage-controlled oscillator (VCO) is inversely proportional to the Q of the LC tank circuit ([2]-[3]). As shown in [4], there is an inverse relation between the noise figure (NF) of a low noise amplifier (LNA) and the inductor Q. Hence, the use of high-Q passives can lead to significant reduction in NF of an LNA. An SOP-based receiver could then contain embedded passives for both the LNA and the VCO whose coupling can lead to system-level issues like feedback and resonance, many of which are not apparent in a System-on-Chip (SOC) implementation.

Ideally, to capture these effects, the system simulation tool should provide for n-port simulations with ports on the boundary as well as internal ports. It should also be computationally efficient, as multiple simulations might be required at the design phase. The authors have attempted to device a design and simulation methodology to analyze the charge concentration and electromagnetic coupling in an active circuit with multiple embedded passives. To study and model the effect of signal coupling, hybrid LNAs using a combination of discrete and embedded passives have been designed for a multilayer organic packaging technology

The paper is organized as follows. Section II describes the design of hybrid LNAs using discrete as well as high-Q embedded passives. It also discusses the effect that coupling between embedded passives have on the amplifier performance. Section III describes two methodologies to model this coupling phenomenon at the design phase. Finally, section IV analyses the findings and outlines future work.

II. Low Noise Amplifier Design and the Effect of Return Current Path on LNA Performance

To study the effect of coupling between embedded passives in a SOP based integration scheme, LNAs with multiple passives were designed and fabricated in a three metal layer organic technology. It consisted of a core substrate of 40mil thick double-sided FR-4 ($\tan\delta = 0.009$ and $\varepsilon_r = 3.7$) with 62.5μ thick epoxy layers of Shipley Dynavia ($\tan\delta = 0.026$ and $\varepsilon_r = 3.2$). The metal (copper) layers were 15μ thick, with 100μ micro-vias.

The classical LNA architecture consists of an active device with impedance transformation networks at the input and output. Fig. 1 shows the schematic of the hybrid LNA, using a discrete HBFP-0420 dual emitter transistor in a SOT-343 package and high Q embedded inductors and capacitors (for the sake of simplicity, the bias circuit has been omitted).

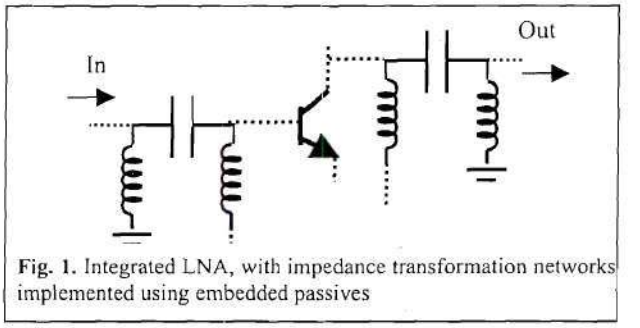

Fig. 1. Integrated LNA, with impedance transformation networks implemented using embedded passives

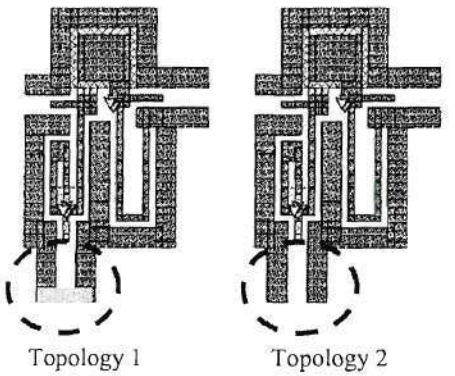

Fig. 2. Two reference ground layout topologies for the input pi. Topology 1 uses a jumper to change the return current path.

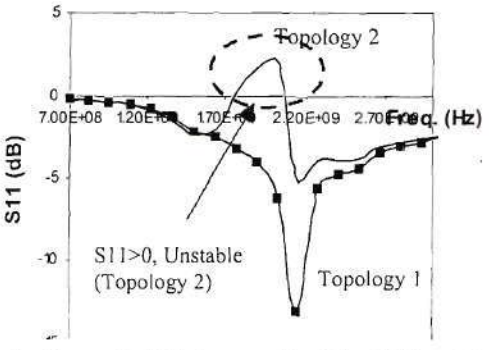

Fig. 3. Change in S11 (measured) of the LNA, with and without the jumpers for charge redistribution.

The input and output of the transistor are matched to 50Ω by using L-C "pi" networks, which are entirely embedded in the package. The pi networks were designed using SONNET. To study the effect of ground return current, pi networks with different reference ground layouts were modeled and implemented, and their effect on the LNA performances was analyzed. Fig. 2 shows two of the topologies used to implement the input pi. Simulations in SONNET gave similar S parameter response for each of these different pi topologies in the 1-3 GHz frequency band. However, Fig. 3 shows the measured response of the amplifier circuits for the two pi topologies, in the same frequency band. The change in routing for Topology 2, caused the amplifier to move into the unstable regime of operation, which could not have been predicted by simply simulating the pi's alone using full-wave solvers.

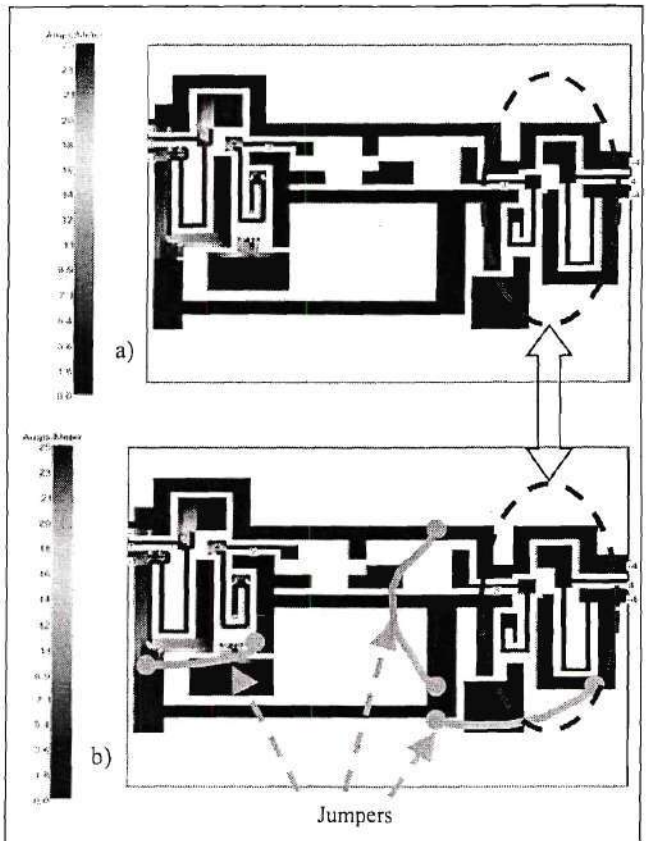

Fig 4. SONNET simulations of the unstable LNA layout at 2 GHz. Circled regions show the problem region, and the change in signal coupling with charge re-distribution. Fig 4a uses an unstable ground layout topology, with significant coupling between input and output pi's. Fig 4b shows the use of jumpers for charge re-routing, and the simulation shows negligible coupling.

Fig. 4a shows SONNET simulations of the complete layout for one of the unstable LNAs (at 2 GHz). The change in the reference ground layout (and hence the return current path) resulted in charge crowding and signal coupling between the input and output pi's. This positive feedback mechanism induces instability in the circuit. The current distribution plots in SONNET showed considerable coupling between the input pi and one of the inductors of the output pi (Fig 4a).

With re-routing of the excess charge to prevent coupling, it was possible to stabilize the amplifier. It is important to note that the second SONNET simulation of the same layout (Fig. 4b), now with better ground routing through the use of jumpers, exhibits considerable reduction in coupled current in the output pi inductors. Through the use of jumpers at appropriate locations, the coupling between the pi networks could therefore be

minimized. The rerouting of the excess charge resulted in the amplifier moving into the stable region of operation.

Table 1 shows the performance summary for two different amplifiers operating in the 2.1 GHz and 2.4 GHz frequency bands. The circuits occupy 1.4 cm^2 in area. The first amplifier, designed for WCDMA applications, shows a gain of 12.74 dB gain and an input match of –14.01 dB at 2.1GHz. The second amplifier, designed for Bluetooth applications, shows a gain of 10.5 dB and an input match of –13.772 dB at 2.4 Ghz.

Table 1. LNA performance summary

LNA	Circuit 1	Circuit 2
Frequency	2.1 Ghz	2.44 GHz
Gain (S_{21})	12.74 dB	10.5 dB
Input Match (S_{11})	-14.01 dB	-13.772 dB
NF (simulated)	2.5 dB	2.8 dB
P_{-1}	-8.9 dB	-9.2 dB
Supply Voltage	3.5 V	3.5 V
Supply Current	7 mA	7 mA

III. Modeling

Though the LNAs could be made operational through the use of jumpers, it is necessary to be able to model the effect of ground return at the design stage itself, so that any system level instability can be identified and rectified at the design stage itself. This involves the incorporation of the reference ground layout in the design and simulation methodology.

A) Field Solvers

Field solvers like HFSS and SONNET can be used to obtain an n-port S parameter file, which can then be used in a circuit based simulation tool like Agilent ADS. However, current modeling tools do have limitations when providing solutions for internal ports, especially devices configured in a CPW topology as was done in this paper.

The effect of the reference ground layout can be modeled as a mutual inductance between the inductors of the input and output pi's, with the coupling coefficient depending on both spatial orientations of the circuit components as well as the return current paths (Fig. 5). The current distribution plots obtained through field solvers can be used to calculate this coupling coefficient. In Fig 4a, the ratio of the current densities in the input and output pi's translated to a coupling coefficient of ~0.2, which, when used in ADS, could model the instability. Similarly, the current distribution plot of Fig. 4b, now with better ground routing through the use of jumpers, exhibits a coupling coefficient of less than 0.05. (In fact, this mutual inductance was required in ADS to completely match the model to the measurement results).

B) Transmission Line Matrix and Coupled Line Theory

Electromagnetic solvers take long computation times, and this further increases as the number of ports is increased. This makes it difficult to use tools like SONNET to model the mutual inductance in circuits at the design phase, when multiple simulations might be required (as changes are made to the layout). To reduce computation time, a circuit based modeling methodology was developed, using coupled-line and transmission line theory.

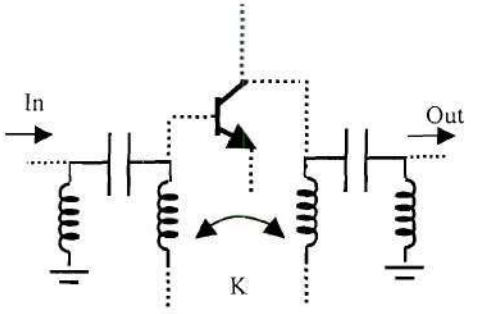

Fig. 5. Integrated LNA, where the coupling due to return current is modeled as a mutual inductance between inductors of the input and output pi's

Modeling each pi network as an equivalent circuit consisting of two inductors and one capacitor makes it impossible to model the effect of the reference ground layout. To solve this problem, the pi's were modeled using coupled line theory [5]. A 2D electromagnetic solver such as ANSOFT 2D provides characteristic mode impedances and propagation constants for lossy and lossless lines. The mode impedances and propagation constants can be used to create a distributed model for the multi-line coupled line sections. The Multilayer T-line models in ADS can also be used to model the passive networks. This process allows the equivalent circuit of the ground layout to be connected to the reference ground of the pi networks. All the signal carrying traces on the substrate that are referenced to coplanar grounds are also modeled as coupled lines.

The reference ground layout was modeled as a mesh of transmission lines referenced to the backside metallization. The size of each transmission line segment is obtained from the maximum frequency of analysis, and is given by $\lambda_{min}/10$.

Fig. 6 shows the equivalent circuit modeling of the LNA. This circuit-based model was able to predict the

instability (Fig. 7), at the same time reducing the computation time by an order of magnitude as compared to modeling using SONNET. Fig. 8 shows a comparison between the measurements (for the stable LNA operating at 2.1 GHz) and modeled data from the two methodologies.

IV. Analysis and Summary

It is to be noted that the circuit-based modeling methodology is valid only at low frequencies (<5 Ghz). The accuracy of coupled-line modeling decreases as the ratio of the wavelength to the thickness of the dielectric increases. The effect of discontinuities is also much higher at high frequencies. In addition, the model has been successful only in predicting the frequency of instability, and not its amplitude.

The effect of coupling in passive networks with CPW topology has been presented here. SONNET simulations for passive networks with microstrip topology show minimal coupling between inductors, as a result of the low-impedance return current path provided by the separate ground plane. However, microstrip inductors typically exhibit lower Q's, necessitating the use of CPW structures for high performance circuits. CPW structures (both with and without conductor backing) exhibit strong coupling that can be removed only through the proper placement of vias (to act as jumpers for charge re-routing), thus proving the need for such a computationally efficient modeling tool.

In summary, a design and simulation methodology to integrate system level full-wave solvers into the design process for active devices with multiple embedded passives has been proposed and validated through measurement results. In addition, a computationally efficient circuit based modeling technique using coupled-line theory has also been developed, to predict the effect of coupling between multiple embedded passives in SOP based integration schemes.

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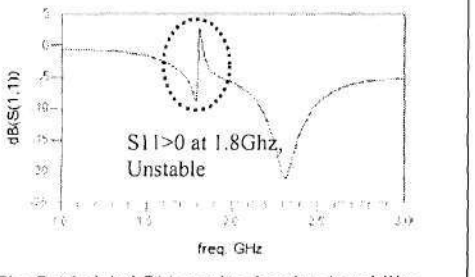
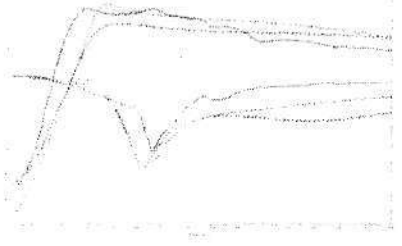


Fig. 7. Modeled S11 results showing instability



Measurement

Modeled Data (simulation in ADS; effect of return current modeled as mutual inductance, calculated using SONNET)

Modeled Data (simulation in ADS; effect of return current modeled using coupled line theory and transmission line network)

Fig. 8. Measurements and modeling results

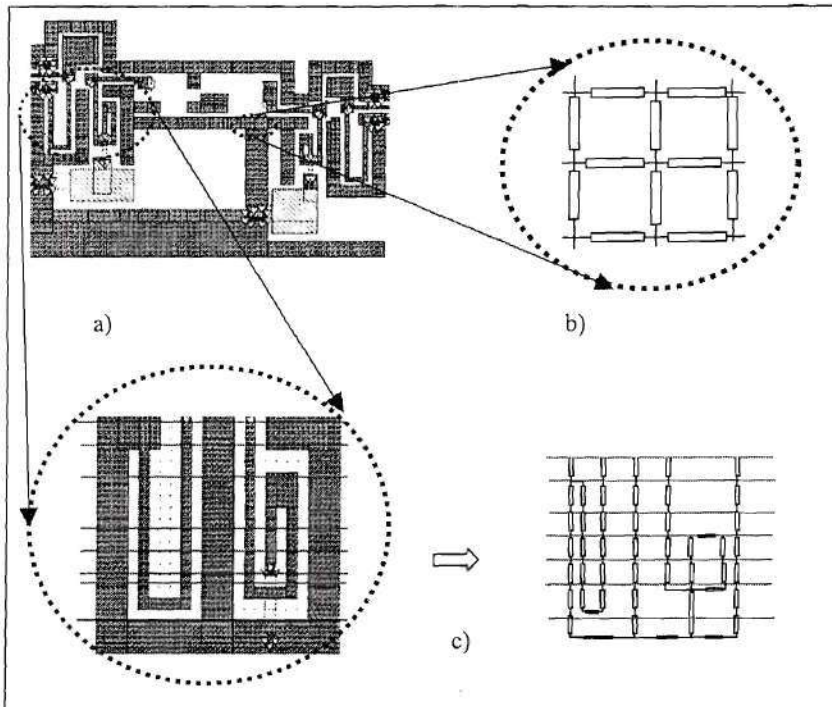


Fig. 6. Equivalent circuit modeling of the low noise amplifier **a)** Layout of the LNA **b)** Transmission line matrix to model the reference ground layout **c)** Segmentation and coupled-line modeling of signal carrying traces and passives networks

DESIGN OF INTEGRATED LOW NOISE AMPLIFIERS (LNA) USING EMBEDDED PASSIVES IN ORGANIC SUBSTRATES

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Keywords – Low noise amplifier (LNA), system-on-package (SOP), integrated passives, embedded inductors, organic packaging, reference ground layout, return current, inductive coupling.

ABSTRACT

The Noise Figure of a Low Noise Amplifier is a function of the quality factor of its inductors. The lack of high-Q inductors in silicon has prevented the development of completely integrated CMOS LNAs for high sensitivity applications like GSM (1.9 GHz) and W-CDMA (2.1 GHz). Recent developments in the design of high-Q inductors (embedded in low cost IC packages) have made single-package integration of RF front-ends feasible. These embedded passives provide a viable alternative to using discrete elements or low-Q on-chip passives, for achieving completely integrated solutions. Compared to on-chip inductors with low Q values and discrete passives with fixed Q's, the use of these embedded passives also leads to the development of the passive Q as a

new variable in circuit design. However, higher Q values also result in new tradeoffs, particularly with respect to device size. This paper presents a novel optimization strategy for the design of completely integrated CMOS LNAs using embedded passives. The tradeoff of higher inductor size for higher Q has been adopted into the LNA design methodology. The paper also presents design issues involved in the use of multiple embedded components in the packaging substrate, particularly with reference to mutual coupling between the passives and reference ground layout.

I. INTRODUCTION

The demand for low-cost wireless solutions has fueled the need for highly integrated systems with communication and computing capabilities. Traditionally, the main means for system integration has been the System-on-Chip (SOC) approach, which requires the implementation of all the functional blocks of a system on a single chip, to reduce cost and improve performance. With improvement in f_T to 50GHz and beyond, the SOC approach using silicon CMOS technology provides the design community with a cost-effective means for implementing the digital and analog sub-blocks of the receiver into a single chip, especially for standards like WLAN where sensitivity requirements aren't very stringent [1]. However, the implementation of the RF front end (consisting of the band pass filter (BPF) and the low noise amplifier (LNA)) in silicon has proved to be an extremely difficult task. This is primarily because of the lack of on-chip high-Q passives.

A survey of work done in this field reveals that typical Qs for on-chip inductors in ordinary silicon CMOS processes tend to be less than 15 (E.g. [2]). The thin aluminum metal layers and the lossy nature of silicon lead to higher parasitics for on-chip inductors,

which makes the design of filters and LNAs for high sensitivity applications like long-distance communication protocols next to impossible. Table 1 ([3]-[8]) shows examples of CMOS LNAs published over the last few years; none of them are completely integrated solutions and they all require external discrete passives for completing the circuit.

Author	Year	Frequency (GHz)	Technology	NF (dB)	Gain (dB)	Completely Integrated?
Karanicolas et al. [3]	1996	0.9	0.5u CMOS	2.2	15.6	NO
Shaeffer et al. [4]	1997	1.5	0.6u CMOS	3.5	22	NO
Hayashi et al. [5]	1998	0.9	0.35u CMOS	1.8	14.8	NO
Floyd et al. [6]	1999	0.9	0.8u CMOS	1.2	14.5	NO
Abou-Allem et al. [7]	2001	1.9	0.5u CMOS	1.8	15	NO
Gramegna et al. [8]	2001	0.9	0.35 RFCMOS	0.85	15	NO

Table 1: Survey of past work on CMOS LNAs for long-distance communications protocols

Developments in packaging technology have led to a second option for integration, the System-on-Package (SOP) approach. Unlike SOC where the package exists just for the thermal and mechanical protection of the ICs, SOP provides for an increase in the functionality of the IC package by supporting multiple chips and embedded passives [9]. Depending on the packaging technology used, there are three main approaches for SOP integration; namely 1) Low-Temperature Co-fired Ceramic (LTCC) (also known as Multi-Chip Module Ceramic (MCM-C)) [10], 2) Multi-Chip Module Deposition (MCM-D) [11] and 3) Multi-Chip Module Laminate (MCM-L) [12]. The dielectric materials and highly conductive copper layers of these packaging substrates makes high-Q embedded inductors and capacitors possible ([10], [12], [13]). This in turn leads to the possibility of implementing completely integrated LNAs at the package level.

Though many papers have reported optimization techniques for CMOS LNAs ([4], [14]), all of them have assumed the use of external inductances with fixed Qs. However, with the use of embedded passives, designers now have the flexibility of choosing the Q required for a particular circuit component and treating it as a new design variable in the optimization process. This paper presents a novel optimization strategy for integrated CMOS LNAs, with simultaneous optimization of transistor and inductor sizing in the IC and the package for minimal noise figure (NF) and device size.

System integration at the package level can lead to the use of multiple embedded passives in the packaging substrate, which can generate undesirable resonance and feedback in the circuit. Due to the small electrical sizes involved, some of these effects can be ignored for on-chip system implementations. Even for issues such as feedback that are common for both on-chip and package implementations, the mechanism for signal coupling can be very different at the chip and package levels. Along with circuit optimization, this paper also analyzes the electrical design issues involved in integrating circuits with multiple passives embedded in a multilayered substrate. To demonstrate the feasibility for integration, LNAs integrated on a multi-layered organic substrate containing embedded passives have been fabricated and tested in this paper.

The paper is organized as follows: Section II discusses the contribution of finite inductor Qs to the NF of a CMOS LNA circuit. Section III provides details on an optimization strategy for LNAs depending on NF and size requirements. Section IV describes the fabrication of embedded inductors in organic packaging substrates and the tradeoffs involved in the design of embedded high-Q inductors. Section V discusses the design of hybrid LNAs using both discrete and embedded components, as proof-of-

concept devices for high-frequency applications as well as test-vehicles to study the effect of coupling between multiple embedded passives. Section VI discusses the effect that mutual coupling between embedded passives and the ground return path layout have on the performance of the LNA and finally, Section VII summarizes the findings and outlines future work.

II. CMOS LOW NOISE AMPLIFIERS AND NOISE ANALYSIS

The low noise amplifier is the first active device of any RF front-end architecture (Fig 1). Essential requirements of this amplifier circuit are reasonable gain, a good input impedance match, linearity and the lowest possible noise figure (NF). If the device is to be used in a portable device, the need for low power consumption also becomes important. The noise factor (F) of an LNA is a measure of the amount of noise added by the circuit to the incoming signal, and is defined as the ratio of Signal-to-Noise Ratio (SNR) at the input of the device to the SNR at the output (1).

$$F = \frac{(SNR)_{in}}{(SNR)_{out}} = \frac{\overline{v_{ni}^2}}{\overline{v_{tx}^2}} \qquad (1)$$

where $\overline{v_{ni}^2}$ is the total noise power at the output referred to the input, and $\overline{v_{tx}^2}$ is the thermal noise power produced by the source resistance (typically 50 Ω). The noise figure is F expressed in dB.

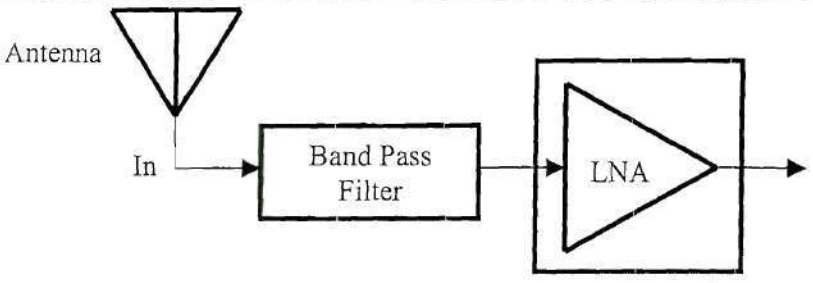


Fig 1. Typical wireless receiver front-end

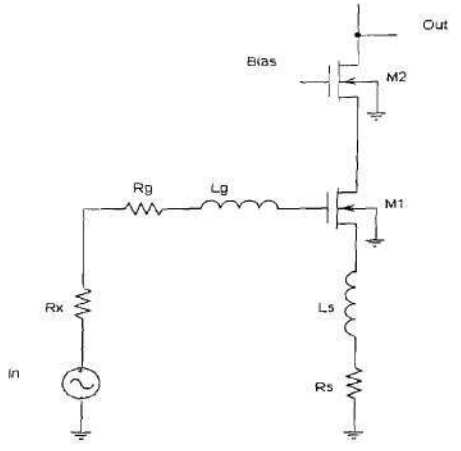


Fig 2. LNA with inductive degeneration. R_g and R_s are parasitic resistances of the inductors L_g and L_s. The bias circuitry has not been shown for simplicity's sake.

Though many topologies exist for LNA design, the cascode architecture of Fig. 2 has been used widely for its low NF and high input - output isolation [4]. The design process for the inductively degenerated LNA consists of sweeping the NF with respect to transistor (M1) gate width. Using the RF CMOS model described in [15], the input impedance of the LNA can be calculated as

$$Z_{in} = R_g + R_s + R_{gate} + R_{ch} + \frac{g_m L_s}{C_{GS}} - jR_s g_m \sqrt{\frac{L_T}{C_{GS}}} + j\omega L_T - \frac{j}{\omega C_{GS}} \qquad (2)$$

where R_g and R_s are the parasitic resistances of the inductors at the gate and source respectively, R_{gate} is the resistance of the polysilicon gate, R_{ch} is the channel resistance, g_m is the transconductance, C_{GS} is the gate-source capacitance, ω is the angular frequency and L_T is the sum of inductances L_s and L_g. If the parasitic resistances (R_g, R_s and R_{gate}) can be ignored, the real part of the input impedance can be controlled by choosing appropriate values for L_s and can be set to equal the source resistance for impedance match. The gate inductance is then chosen such that L_T resonates with C_{GS} at the operating frequency, thus canceling out all the imaginary terms and making the input impedance purely real at the frequency of operation.

Inductances can be modeled as equivalent circuits comprising of inductors, capacitors and resistors. The energy stored in the device is shared between the inductance and the parasitic capacitances, while the resistor represents the loss in the device. As such, the unloaded Qs of the inductors are functions of the parasitic capacitances as well as the resistance. If the parasitic capacitances are very small and can be neglected, the unloaded Qs (Q_g and Q_s) of the inductors (L_g and L_s) are related to their parasitic resistances by

$$R_g = \frac{L_g \omega_0}{Q_g} \qquad R_s = \frac{L_s \omega_0}{Q_s} \qquad (3)$$

where ω_0 is the angular frequency of operation.

As mentioned earlier, several papers have discussed optimization strategies for CMOS LNAs ([4], [14]). All of these design methodologies have assumed fixed Qs for the inductors. An SOP approach that provides embedded inductors in the package substrate allows the designer an extra design variable, namely, the Q of the inductors. Depending on their contribution to performance specifications like NF and gain, any or all of the three inductors in the LNA circuit can be implemented on-chip or embedded in the package. However, attaining a particular Q also comes with tradeoffs in size and layout. In order to incorporate these into the optimization methodology, it is necessary to derive F as a function of R_g and R_s.

The output current of the LNA (i_o) can be defined as

$$i_o = G_{mg}(v_i + v_{ng}) + G_{ms}v_{ns} + A_{ig}i_{ng} + A_{id}i_{nd} \tag{4}$$

where v_i is the input voltage, v_{ng} is the total noise voltage at the gate, v_{ns} is the total noise voltage at the source, and i_{ng} and i_{nd} are the gate and drain noise currents of the transistor M1. In the above equation, G_{mg}, G_{ms}, A_{ig} and A_{id} are the system gains associated with the different voltage and current sources respectively. Since the output current i_o is also given by

$$i_o = G_{mg}(v_i + v_{ni}) \tag{5}$$

(where v_{ni} is the total noise voltage in the FET referred to the input), combining equations (4) and (5) results in

$$v_{ni} = v_{ng} + \frac{G_{ms}}{G_{mg}}v_{ns} + \frac{A_{ig}}{G_{mg}}i_{ng} + \frac{A_{id}}{G_{mg}}i_{nd} \tag{6}$$

Including all the noise contributions of the FET and that of the parasitic resistances of the inductors, F can then be derived from (1) as [16]

$$F = 1 + \frac{R_g}{R_x} + \frac{R_{gate}}{R_x} + \frac{R_s}{R_x} + \frac{\beta \omega_0{}^2 C_{GS}{}^2 (\omega_0{}^2 L_T{}^2 + (R_x + R_g + R_{gate} + R_s)^2)}{5 R_x g_{do}}$$
$$+ \frac{2c\omega_0{}^2 C_{GS}{}^2 (R_x + R_g + R_{gate} + R_{ch} + R_s)(R_x + R_g + R_{gate} + R_s)}{g_m Rx} \sqrt{\frac{\beta\gamma}{5}}$$
$$+ \frac{\omega_0{}^2 C_{GS}{}^2 (R_x + R_g + R_{gate} + R_{ch} + R_s)^2}{g_m{}^2} \frac{\gamma g_{do}}{R_x} \qquad (7)$$

where R_x is the source resistance, which is typically 50Ω, β and γ are bias dependant noise parameters of the MOSFET and g_{do} is defined as the drain output conductance evaluated at Vds=0V. In (7), c is the correlation coefficient between the drain and gate noise currents of the FET.

III. DESIGN OPTIMIZATION

Equation (7) shows that F is equally dependent on the parasitic resistances of both gate and source inductors (R_g and R_s). However, in practice, L_s is much smaller than L_g. Values of inductance required for L_s are typically less than 2nH, and this can be implemented as an on-chip or bond-wire inductance whose parasitic resistance can be neglected. By careful layout, the resistance of the polysilicon gate can also be made very small [4]. However, depending on the frequency of operation, L_g can be as high as 35 nH. The parasitic resistance of L_g (R_g) is hence a very important contributor to the F of the LNA. As it is impossible to implement this inductor on-chip, an optimum solution is to embed it in the package.

Fig. 3 shows the variation of NF with respect to transistor gate width (W), for different values of Q_g, for a 1.9 GHz CMOS LNA designed for the AMI 0.5μ process. As

can be observed, there exists an optimum gate width where the NF is minimum. However, this minimum NF shifts upwards as the value of Q_g is decreased. It is also important to note that this change is not a linear function of Q_g; *the improvement in NF with an improvement in* Q_g *is much more apparent at low values of* Q_g. Current design methodologies suggest designing circuits assuming infinite Q, and then using inductors with highest possible Q. This is not a very satisfying strategy, as there are always tradeoffs involved in achieving high Qs during inductor design. The non-linear variation of *NF* with Q_g provides the scope for an optimization methodology.

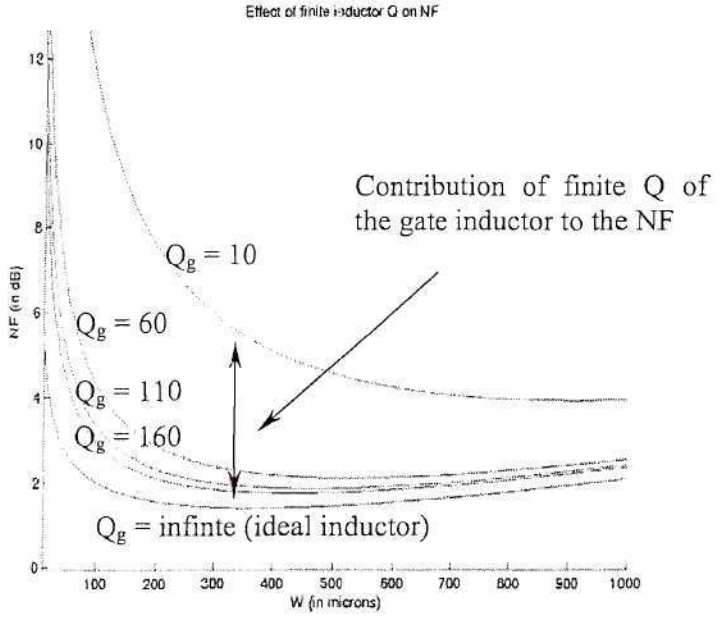


Fig 3. Variation of *NF* with transistor width (for different values of Q_g), for a 1.9 GHz CMOS LNA designed for the AMI 0.5μ process.

The Q of an inductor is a function of the signal loss within the device. The losses in an inductor consist of two components, namely, losses in the metal and losses in the substrate. It has been shown in [12] that the inductor can be optimized for maximum Q at

the frequencies of interest (1-3 GHz). Under these conditions, conductor losses dominate the total loss (and hence the Q). The conductor losses can be reduced by increasing the metal thickness and conductor width (which reduces the series resistance), leading to an increase in size of the inductor, thus allowing for the tradeoff of larger size for higher Q.

By using embedded inductors in place of chip-inductors for L_g, the designer has control over the required unloaded Q for this inductor. However, due to the tradeoff with respect to size, using inductors with the maximum Q possible is not a good strategy and could lead to unnecessarily large sizes for the packaged LNA.

Equation (7) can be used to find the optimum Q_g, required for a particular *NF*. Fig. 4 shows the variation of *NF* for the optimum transistor gate width. *NF* decreases rapidly for increasing Q_g at low values of Q_g, but the rate of change decreases at higher values of Q_g. *Hence, there is very little reduction in NF beyond a certain inductor Q.* Equation (7) and Fig. 4 provides the minimum tolerable inductor Q required for satisfying the sensitivity requirements of a particular circuit. For protocols like Bluetooth and WLAN where the NF requirements are comparatively relaxed, even a Q of 25 is sufficient to achieve a NF < 3.5 dB. Higher Qs (60-80) are required to meet the specs of long distance communication protocols like GSM and WCDMA.

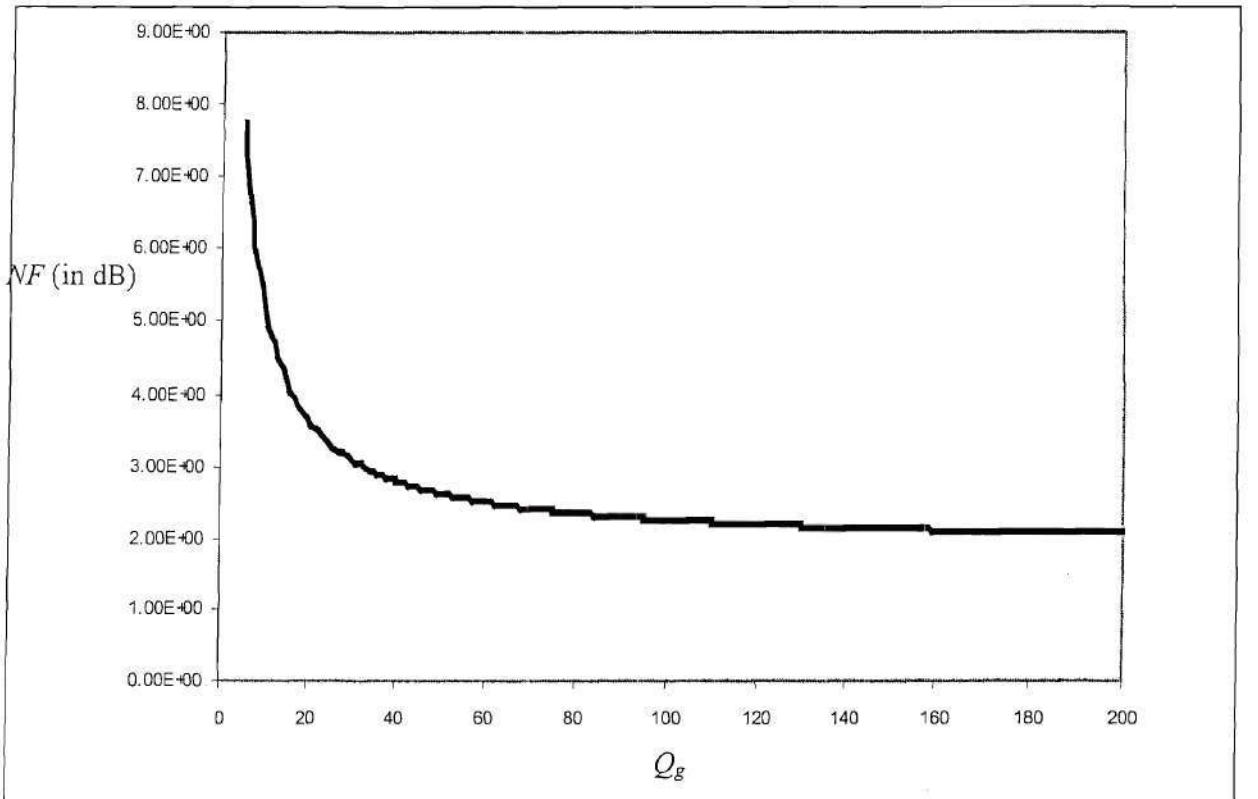


Fig 4. Variation of *NF* with Qg, for a 1.9 GHz CMOS LNA designed for the AMI 0.5μ process.

Taking the partial derivative of F (in Equation (7)) with respect to Q_g, results in:

$$\frac{\partial F}{\partial Q_g} = -\frac{L_g \omega_0}{Q_g^{\,2}} \left[\begin{array}{l} \dfrac{1}{R_x} + (2K_1 + K_3)(R_x + R_{gate} + R_s + \dfrac{L_g \omega_0}{Q_g}) \\ + (2K_2 + K_3)(R_x + R_{gate} + R_{ch} + R_s + \dfrac{L_g \omega_0}{Q_g}) \end{array} \right] \quad (8)$$

where

$$K_1 = \frac{\beta \omega_0^{\,2} C_{GS}^{\,2}}{R_x g_{do}} \qquad K_2 = \frac{\gamma g_{do} \omega_0^{\,2} C_{GS}^{\,2}}{R_x g_m^{\,2}} \qquad K_3 = \frac{2c\omega_0^{\,2} C_{GS}^{\,2} \sqrt{\gamma\beta}}{R_x g_m} \quad (9)$$

Equation (8) can be used to find the optimum Q_g required, at which the rate of decrease of NF meets a certain value.

IV. EMBEDDED PASSIVES – OPTIMUM Q WITH MINIMUM SIZE

Embedded inductors and capacitors have been demonstrated on MCM-L technology developed at the Packaging Research Center, Georgia Institute of Technology [12]. The PWB/packaging substrate on which these devices were fabricated was processed by laminating a low-cost epoxy based layer, Dupont Vialux™, on a conventional 28 mil (~700um) printed wiring board (PWB) core, N4000-13™. This resulted in a two-metal layer process, which was sufficient for the design of parallel plate capacitors and under-routing capabilities. The process also offers microvias (with 100μm diameters), which are important for the realization of minimum size passives in multi-layered substrates. The 1st metal layer thickness was limited to half the laminate layer thickness of 25um for ensuring a uniform dielectric layer thickness. The top metal layer was restricted to 15~17um to ensure uniform metal thickness. The vendor supplied data for the two layer substrate were as follows: Dupont Vialux™ had a dielectric constant of 3.3 and loss tangent of 0.015 at 1 GHz and N4000-13™ had a dielectric constant of 3.7 and loss tangent of 0.015 at 1 GHz. Fig. 5b shows the cross-section of the substrate.

Inductors and capacitors were optimized for maximum Q at the appropriate frequency. Figure 5a shows the top view of a 4"x 4" quadrant of the substrate with inductors and capacitors. Table 2 provides measured results for passives realized in the above technology. Microstrip type inductors use signal lines referenced to a ground directly underneath the device. With the given organic process, it was possible to have minimum line widths of 3 mils and a maximum ground to signal separation of 29 mil

(Figure 5b). In co-planar waveguide (CPW) inductors, signal lines are referenced to ground rings on the same metal layer as the device. Although this eliminates the need for backside connections, it results in an increase in the area of the device. The CPW topology reduces current crowding on the ground planes (which is typical in microstrip type inductors), by forcing the currents to flow around the device in the larger area coplanar ground. Inductors with Qs as high as 170 have been demonstrated, as shown in Table 2.

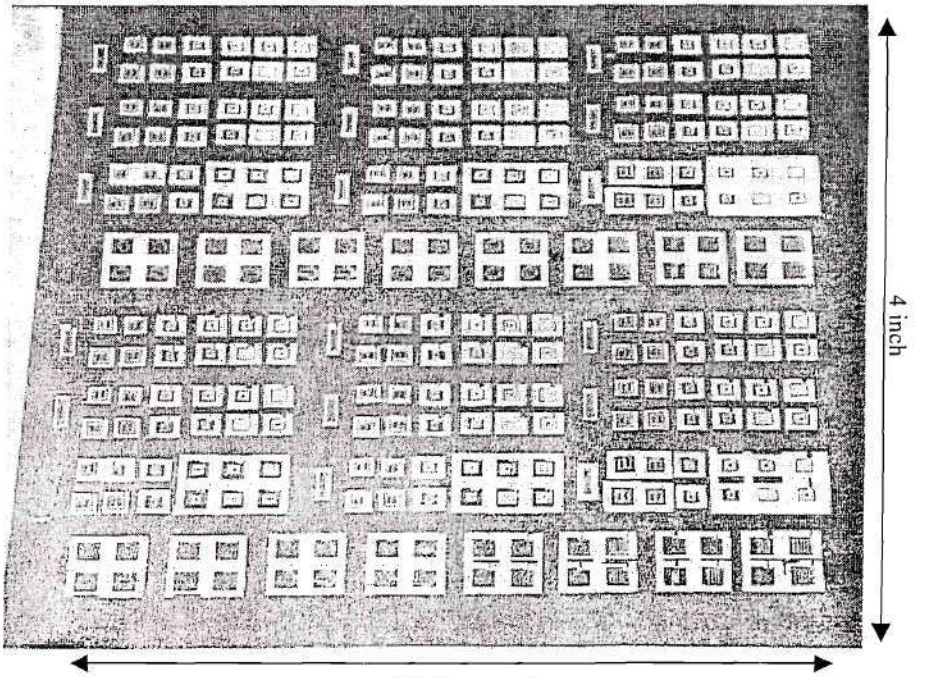
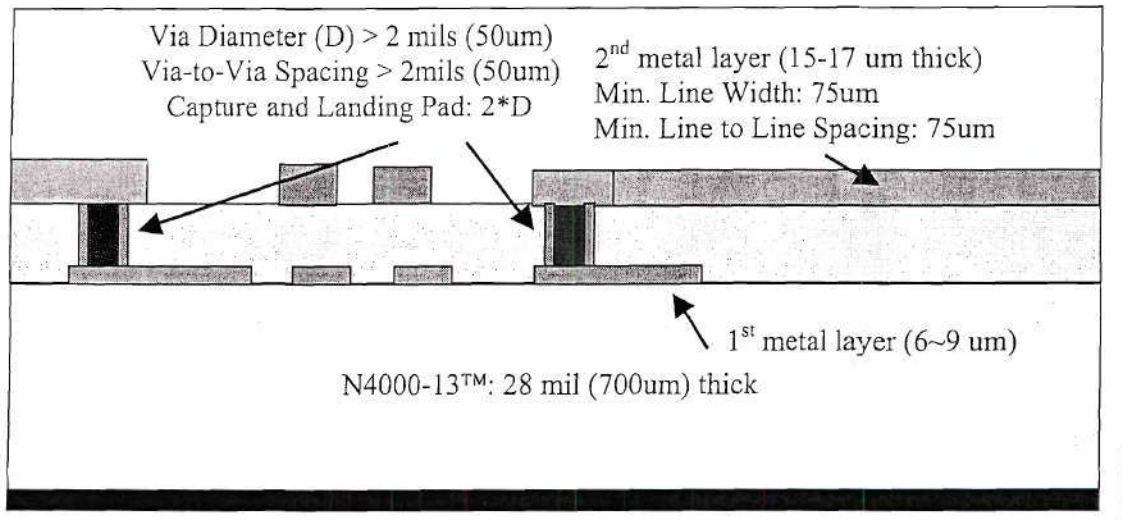


Fig 5. a) Photograph of fabricated passives



b)

Fig 5b) MCM-L substrate cross-section.

Inductors	Max Q	Inductance	SRF	Area (mm^2)
CPW Circular Large	160 @ 1.8 GHz	16nH	>3.6GHz	25
CPW Circular Small	170 @ 2.2 GHz	9nH	>4.5GHz	28
1 turn microstrip	170 @ 2.4 GHz	1.6nH	>5GHz	3.5
2 turn microstrip	110 @ 2 GHz	5nH	> 5GHz	4.1
3 turn microstrip	100 @ 1.2 GHz	12nH	>3GHz	3
1.75 loop microstrip	110 @ 2.1 GHz	7.7nH	>4.3GHz	4
2 loop CPW	110 @ 1.8 GHz	9nH	>3.6GHz	9
2by2 loop CPW	80 @ 1.8 GHz	14nH	>3.6GHz	9
1.75 loop CPW	150 @ 2.2 GHz	5 nH	>4.5 GHz	9
Capacitors	**Q at 2GHz**	**Capacitance**	**SRF**	**Area (mm^2)**
Parallel Plate	33	0.92pF	>6GHz	0.6
Parallel Plate	30	1.78pF	>6GHz	1.16
Parallel Plate	28	2.72pF	>5GHz	1.87

Table 2: Measurement results for passives on organic substrates

Lumped model equivalents for 1-port inductors fabricated using the organic process are shown in Fig. 6. The series inductance, Ls, and the series resistance, Rs, represent the inductance and resistance of the inductor and under-routings respectively.

The overlap between the inductor and the underpass allows direct capacitive coupling between the two terminals of the inductor. This feed-through path is represented by the series capacitance Cs. Components Cp and Rp capture the shunt capacitance and conductance between the inductor and the ground reference.

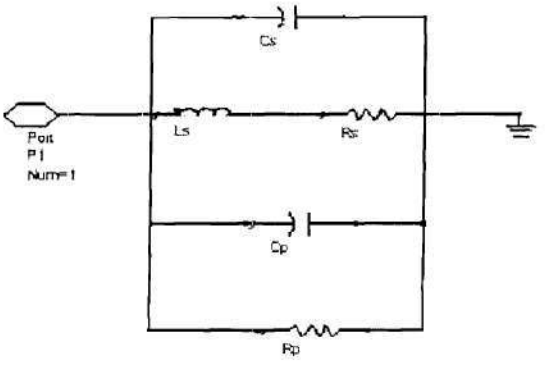


Fig 6. Inductor lumped-element model.

Table 2 also provides measurement results for parallel plate capacitors. Compared to the inductors, the capacitors exhibit lower Q values. This is because the upper limit for the Q factor for any size capacitor implemented on this substrate at a particular frequency, ignoring conductor loss, can be approximated using 1/tanδ, where tanδ is the loss tangent of the material at the particular frequency. The Q factor is further reduced by the conductor loss. Compared to the dielectric materials used in common LTCC (tanδ of 0.0015 at 10 MHz [10]) and MCM-D (tanδ ~ 0.0008 [11]) processes for embedding passives, the materials used in this build-up process are lossy (tanδ ~ 0.015). This sets the maximum Q possible for capacitors in the process at ~ 65.

The variation in Q for two inductors with the same topology and inductance but different areas can be explained based on the model of Fig. 6 - the smaller inductor has

larger series resistance and smaller parallel resistance compared to the larger inductor, and this results in a lower value of Q for the smaller inductor. An inductor can be made smaller by increasing its proximity to the reference ground. However, this directly decreases the inductance per unit length due to the negative mutual inductance with the ground plane. Thus, there is an increase in series resistance for a smaller inductor due to the increase in the length required to achieve the same inductance compared to a larger inductor.

Fig. 7 shows photograph of a spiral inductor fabricated on an organic substrate (the CPW ground ring around the inductor is not been shown in the figure). There are several design variables for this inductor topology, namely the inner diameter, distance between the signal trace and the CPW ground, trace width, spacing between traces and number of turns. As an example to demonstrate the variation of Q with inductor area, three single-turn inductors were designed for the same inductance (~7.8nH) value. Table 3 shows the area and Q (measured at 1.83 GHz) for these inductors. As can be observed, for a given topology (inductor shape and number of turns), there is an increase in Q with increase in device area.

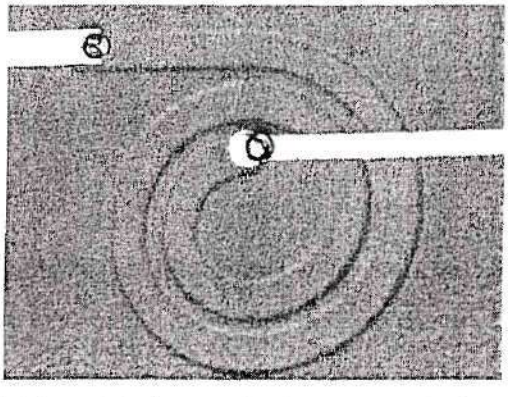


Fig 7. Photograph of the fabricated inductor (the CPW ground ring around the inductor is not shown)

Inductance (nH)	Q	Area (mm^2)
7.81	48.81	14.747
7.82	70.897	17.743
7.81	85.52	18.92

Table 3: Variation of inductor Q with area,

Fig. 8 shows the variation of inductor area and *NF* with Q_g, for an LNA designed using these inductors. The dotted line represents the specification for NF, which in this case was 2.5 dB. The NF vs. Qg curve shows that the minimum inductor Q required to meet this specification is 64. The Area vs. Qg curve is then used to determine the minimum size for the inductance that provide this Q (which in this case was ~17 mm^2).

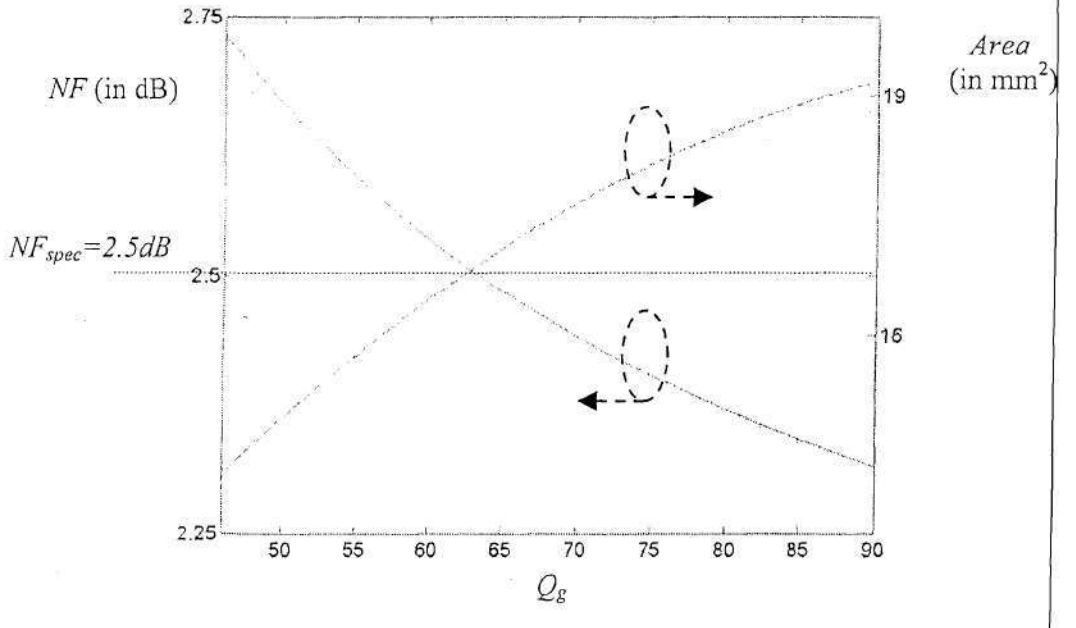


Fig 8. Variation of inductor area and *NF* with *Qg*.

As an example of the chip-package co-design methodology discussed in this paper, an LNA for GSM applications was designed for AMI's 0.5μ CMOS technology, with a standard source resistance of 50Ω and an operating frequency of 1.9 GHz, leading to inductance values of 9 nH and 1.2 nH for L_g and L_s respectively. L_s was small enough to be implemented on-chip; however, L_g was too high to be implemented on-chip without a drastic increase in the NF of the circuit. Plotting the NF of the LNA versus its gate inductor Q, the NF decreases from about 5.2 dB to 2.1 dB as the Q of the gate inductor is increased from 10 to 200. However, on designing, fabricating and measuring different topologies for the gate inductance, it was found that its size increased from $9mm^2$ for a Q of 110 to 28 mm^2 for a Q of 170. Since the NF of the LNA was not affected for an increase in Q_g beyond 70-90 and since size constraints limited the packaged device to an area of 3.5mm x 3.5mm, the inductor that provided optimum Q for a minimum size was chosen.

Fig. 9 shows the package layout of the proposed LNA, along with simulated gain and NF numbers. The embedded inductor has a 2-loop CPW topology, occupies 9 mm^2 of area and has a Q of 110. The package uses a six metal layer organic packaging technology, with the inductor designed using metal layers 2 and 3. Metal layer 1 contains pads for chip attachment. The components of the equivalent circuit model (Fig. 6) for this inductor were extracted from measurements, which translate to a series inductance (Ls) and resistance (Rs) of 7.4 nH and 0.4Ω respectively, and a parallel resistance (Rp) and capacitance (Cs + Cp) of 27 kΩ and 0.15 pF respectively. Fig. 9b shows the measured variation in Q with frequency for this inductor. It is important to note that this data has been obtained using inductors fabricated on lossy organic substrates.

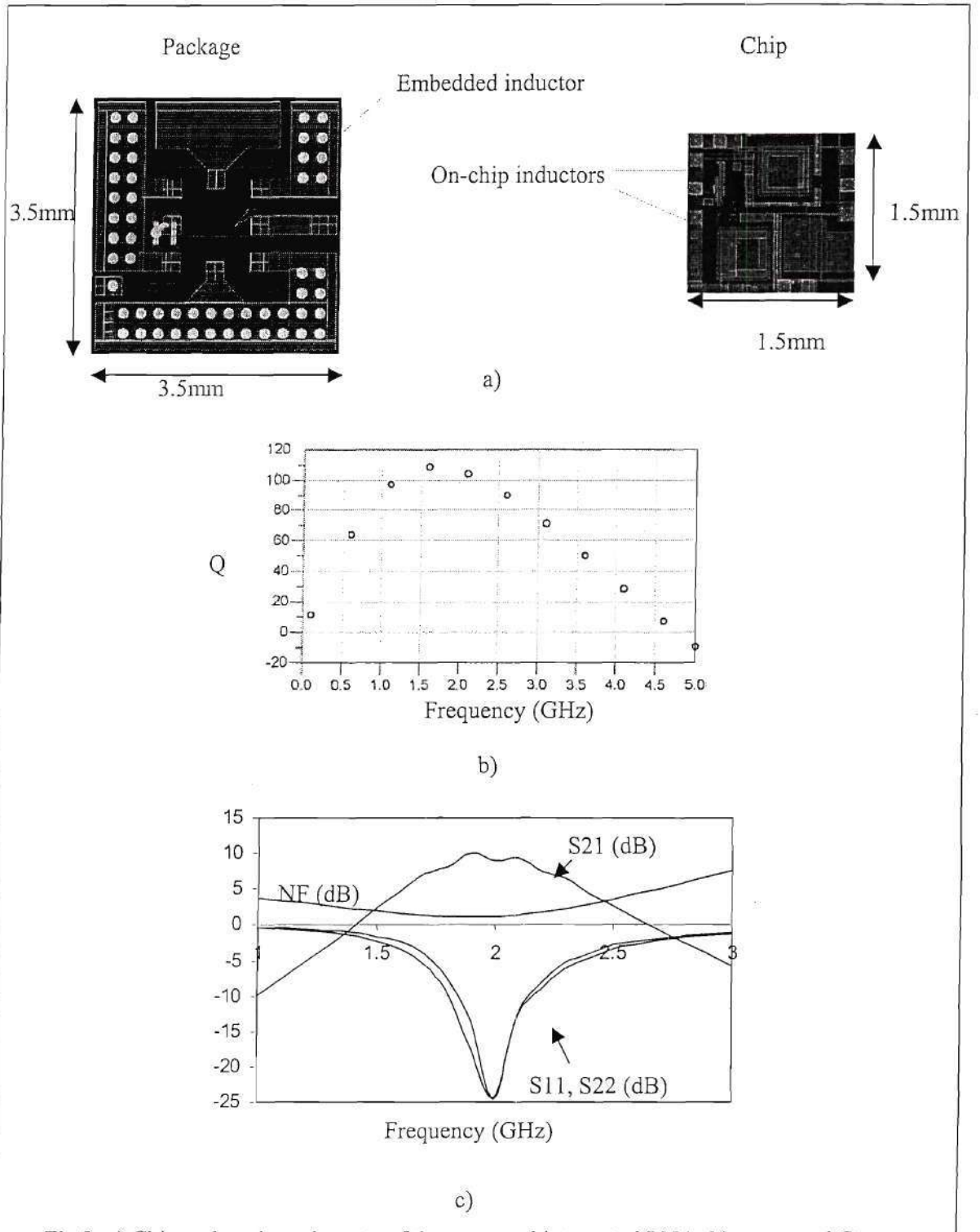


Fig 9. a) Chip and package layouts of the proposed integrated LNA, **b)** measured Q values for the inductor used (9 nH, 2-loop CPW topology) and **c)** simulated gain and NF numbers.

V. HYBRID LNA DESIGN AND MEASUREMENTS

With higher levels of system integration, multiple passives embedded in the package are necessary. For example, the phase noise of a voltage-controlled oscillator (VCO) is inversely proportional to the Q of the LC tank circuit ([17], [18]). An SOP-based receiver could then contain embedded passives for both the LNA and VCO. As mentioned earlier, multiple embedded passives in the package leads to system-level issues like feedback and resonance, many of which are not apparent in an SOC implementation. To study these and as proof-of-concept devices for the use of embedded passives in organic technology for high-frequency applications, hybrid LNAs using a combination of discrete and embedded passives were designed for the packaging technology described in the previous section. The circuits were designed for use in the 2.1 GHz and 2.4 GHz frequency bands.

The classical LNA architecture consists of an active device with impedance transformation networks at the input and output. The NF is mainly affected by the noise characteristics of the transistor and the input impedance matching network. Generally, the source impedance required by the active device for minimum NF is different from the complex conjugate of the input impedance obtained looking into the base/gate of the device (the optimum impedance for maximum power transfer). This means that it is usually not possible to simultaneously achieve both maximum gain and minimum noise figure for an amplifier, and that some compromise has to be made. In addition to gain and NF, stability is also an important factor in amplifier design. This again requires careful choice of source and load impedances, so that the amplifier does not move into the unstable region of operation. The selection of the optimal source impedance Z_{opt} is

achieved by plotting constant NF circles and constant gain circles along with stability circles on a Smith chart. The input impedance transformation network transforms the source impedance (typically 50Ω) to Z_{opt}. The output impedance transformation network transforms the impedance at the collector/drain of the active device to 50Ω for maximum power transfer.

Fig. 10 shows the schematic of the LNA, using a discrete HBFP-0420 dual emitter transistor in a SOT-343 package and the impedance transformation networks implemented using high-Q embedded inductors and capacitors. The transistor is biased in the common emitter configuration.

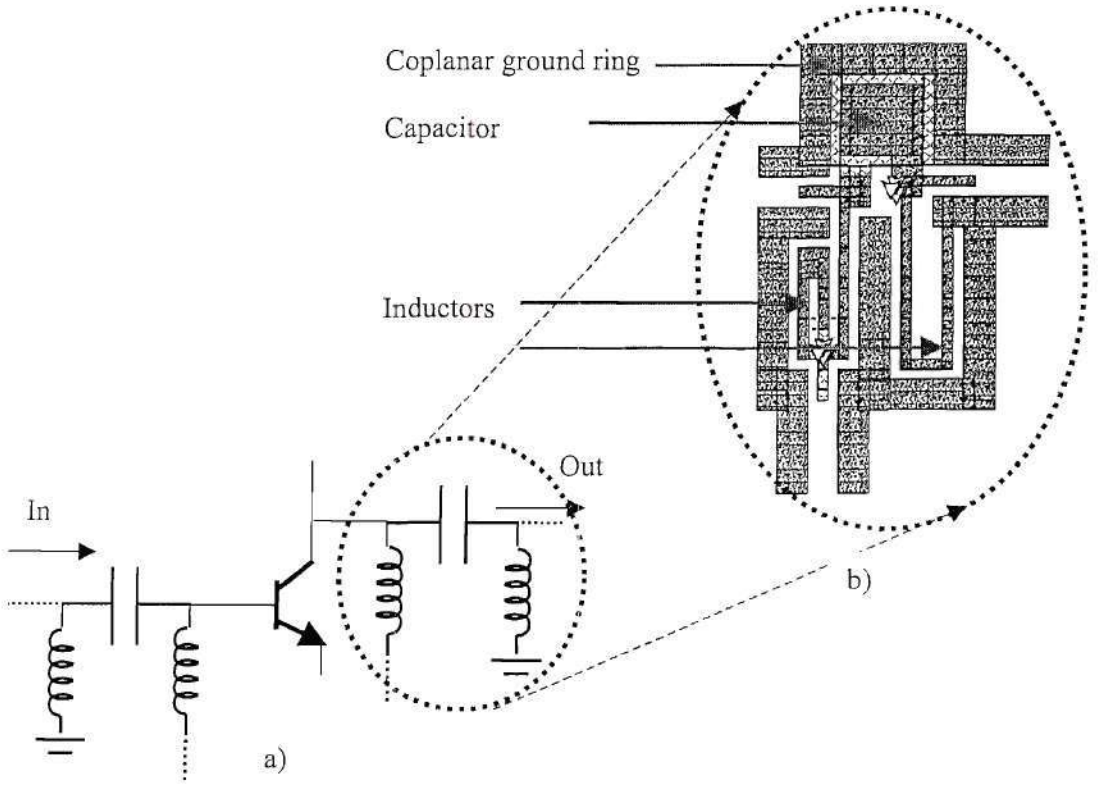


Fig 10a. LNA with impedance transformation networks (pi networks). b) Implementation of the output pi using embedded passives.

The input and output of the transistor were matched to 50Ω by using L-C pi networks, which were embedded in the package. Though "L" networks are sufficient for a narrow-band impedance transformation, the goal was to study the layout issues and interaction between multiple embedded passives. A decision was therefore taken to maximize the number of embedded devices in the system. The output pi was designed for maximum power transfer, and thus performs impedance transformation from the complex conjugate of the collector impedance to 50Ω. The input pi was designed for minimum noise figure, and presents the Z_{opt} to the gate of the transistor.

The pi networks were designed using SONNET, which is a commercial 2.5D method-of-moments solver. As shown in [16], unloaded Q's of 60-80 for the passives were sufficient to attain near-minimum noise figure. Although Q's greater than 150 were achieved in [13], the designs occupied >9mm^2 of the surface area. The design of inductors in this paper was constrained to a maximum surface area of 2mm^2 and the overall pi area to less than 6mm^2.

Fig. 11 shows the layout and the photograph of one of the fabricated LNAs, as well as the measured gain (S_{21}) and impedance match (S_{11}) values for two different amplifiers operating in the 2.1 GHz and 2.4 GHz frequency bands. The circuits occupied 1.4 cm^2 in area. The first amplifier, designed for WCDMA applications, shows a gain of 12.74 dB gain and an input match of –14.01 dB at 2.1GHz. The second amplifier, designed for Bluetooth applications, shows a gain of 10.5 dB and an input match of –13.772 dB at 2.4 Ghz. The plots show good correlation between measured and modeled data. However, as will be explained in more detail in the next section, it was necessary to

account for coupling between the input and output pi's to achieve the results shown. Table 4 shows the performance summary of the two amplifiers.

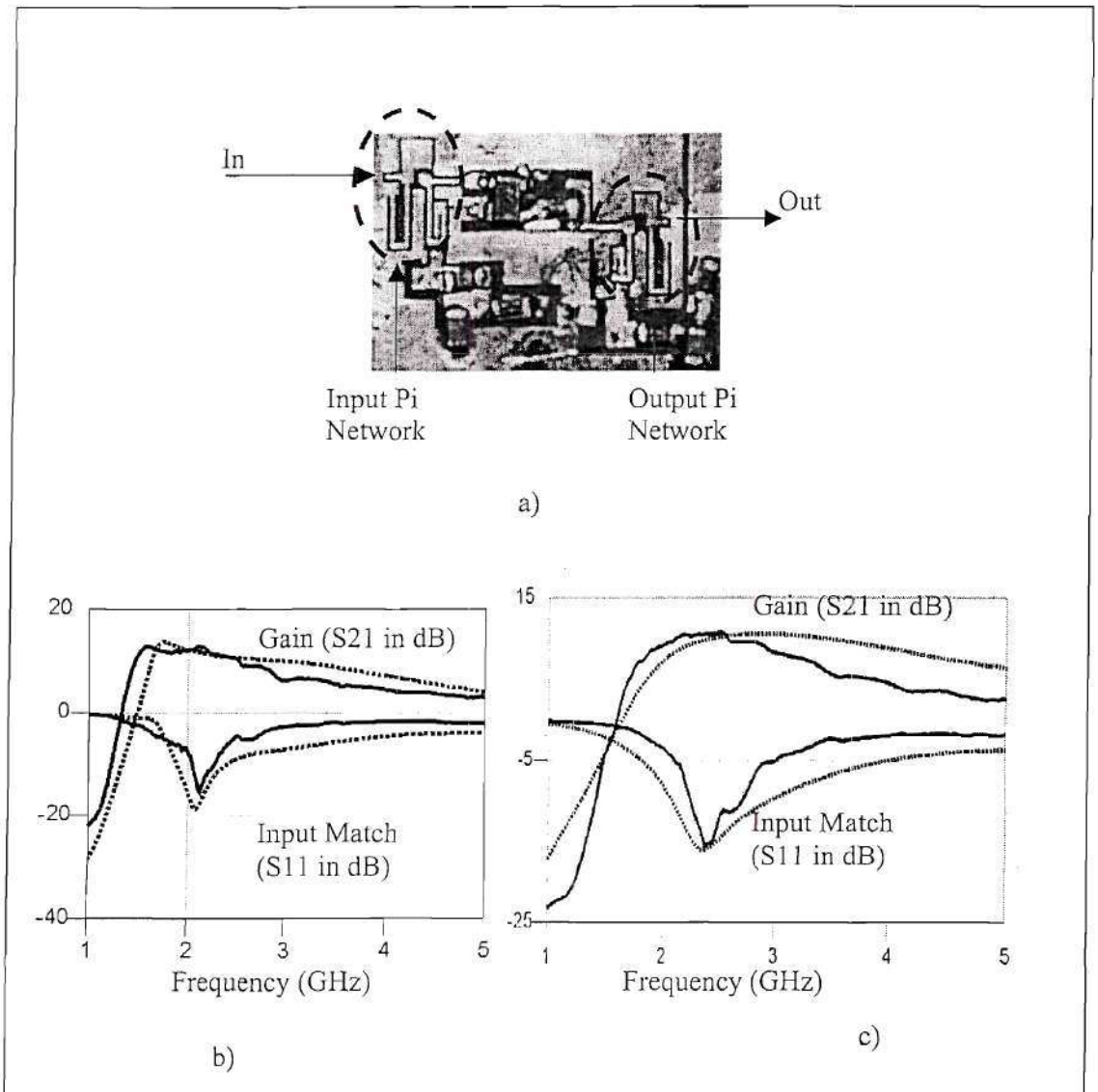


Fig 11. a) Photograph of a fabricated LNA **b)** and **c)** Modeled and measurement data for LNAs operating at 2.1 GHz and 2.4 GHz respectively (the dotted line represents the modeled data and the continuous line represents the measured values).

LNA	Circuit 1	Circuit 2
Frequency	2.1 Ghz	2.44 GHz
Gain (S_{21})	12.74 dB	10.5 dB
Input Match (S_{11})	-14.01 dB	-13.772 dB
NF (simulated)	2.5 dB	2.8 dB
P_{-1}	-8.9 dB	-9.2 dB
Supply Voltage	3.5 V	3.5 V
Supply Current	7 mA	7 mA

Table 4: LNA performance summary

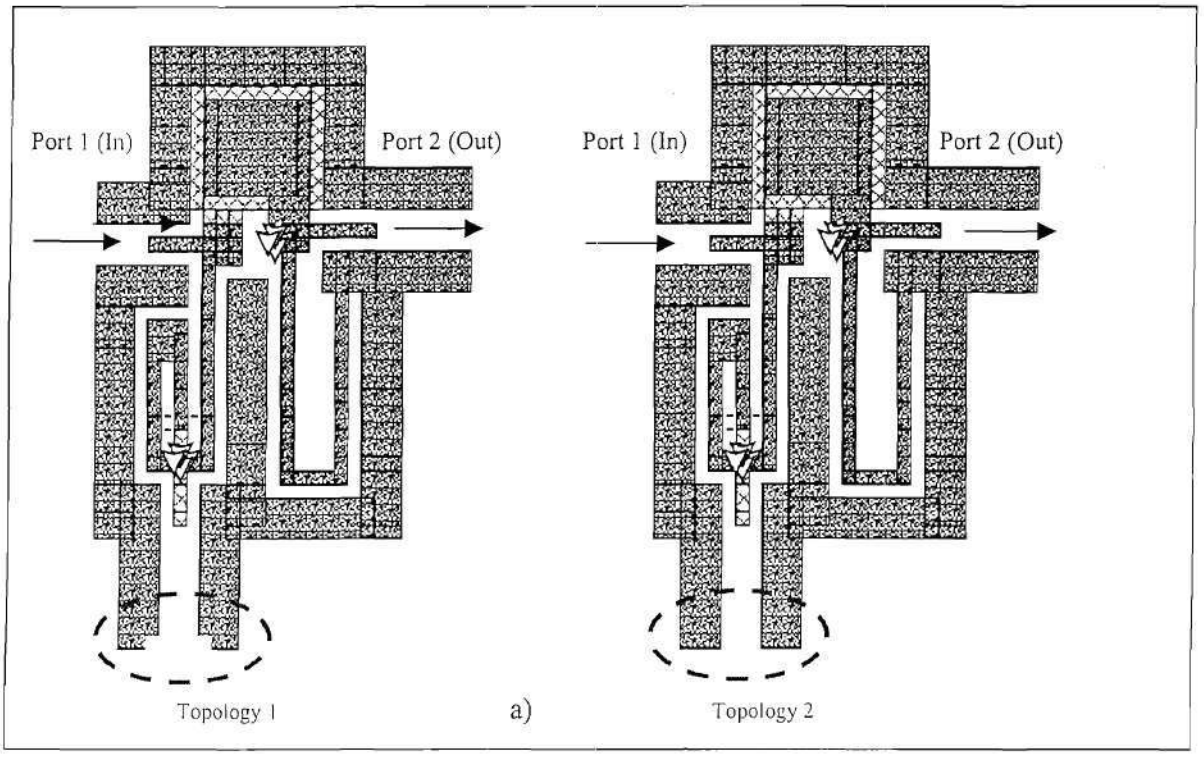
VI. IMPORTANCE OF GROUND RETURN

Circuits with multiple passives have the problem of coupling between the passives. This can lead to feedback, instability and an overall degradation of the circuit performance. In circuits where passives are in close proximity (inside a chip, for example), coupling is mostly magnetic in nature [19]. However, in electrically larger circuits like the LNAs described above, the passives are sufficiently far apart to prevent direct magnetic coupling. Feedback is mostly caused by return currents in such cases. In either case, the relative placement of the passives and their reference grounds becomes a crucial design issue.

To study the effect of ground return current, pi's with different reference ground layouts were modeled and implemented, and their effect on the LNA performances was analyzed. Fig. 12a shows two of the topologies used to implement the output pi and Fig. 12b shows the SONNET simulations for both the pi layouts. As can be observed (in Fig. 12b), for the frequency band of interest, there is minimal difference in the S-parameters for the two topologies. However, Fig. 13 shows the measured response of the amplifier circuits for the two pi topologies. The change in routing for Topology 2, caused the amplifier to move into the unstable region of operation, which could not have been

predicted by simply simulating the pi's alone using full-wave electromagnetic solvers. The instability is caused due to the influence of return currents on the transistor circuit.

With layout of the reference ground resulting in such drastic changes in system performance, it becomes necessary to model its effect at the design stage, so that any system level instability problems can be identified and rectified. This involves the incorporation of the reference ground layout into the design and simulation methodology.



b)

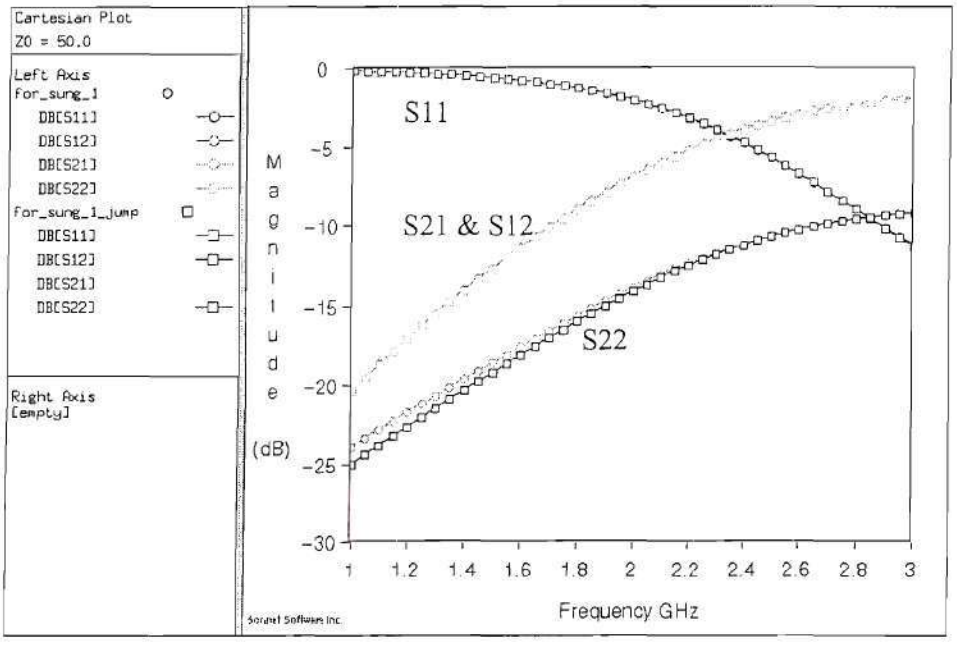


Fig 12. a) Two reference ground layout topologies for the output pi. **b)** SONNET simulations for both layouts.

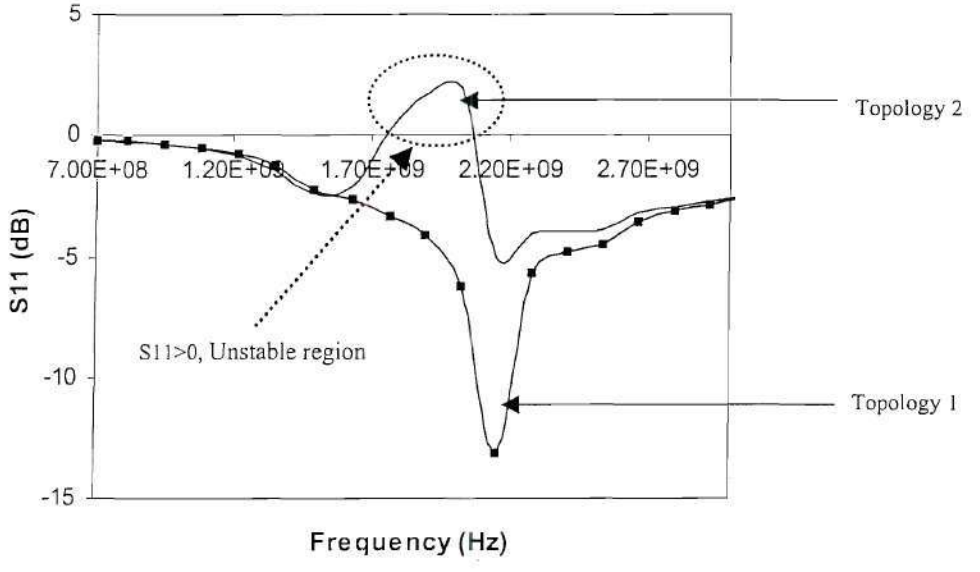


Fig 13. Measured S11 values for the two pi topologies of Fig. 12a, showing the effect of the reference ground layout on LNA performance.

A) Modeling - Field Solvers

Field solvers like HFSS and SONNET can be used to obtain an n-port S parameter file for the entire layout, which can then be used in a circuit based simulation tool like Agilent ADS. However, current modeling tools do have limitations when providing solutions for internal ports, especially for devices configured in a CPW topology as discussed in this paper. Instead, the effect of the reference ground layout can be modeled as a mutual inductance between the inductors of the input and output pi's, with the coupling coefficient depending on both spatial orientation of the circuit components as well as the return current paths.

SONNET simulations of the complete layout for the unstable LNA. showed considerable coupling between the input pi and one of the inductors of the output pi. The reference ground layout (and hence the return current path) for pi Topology 2 resulted in current crowding and signal coupling between the input and output pi's, leading to positive feedback and instability. The ratio of the current densities in the input and output pi's translated to a coupling coefficient of ~0.2, which, when used in ADS, modeled the instability (Fig 14a and 14b). With re-routing of the excess current to prevent coupling (through the use of jumpers), it was possible to stabilize the amplifier. It is important to note that the second SONNET simulation of the same layout (Fig. 15), now with better ground routing through the use of jumpers, exhibits a coupling coefficient of less than 0.05. Measured results for this LNA showed stable operation and a gain of 12dB at 2.1 GHz, proving that the instability in the earlier case was indeed because of return current routing. Through the use of jumpers at appropriate locations, the coupling between the pi networks could therefore be minimized.

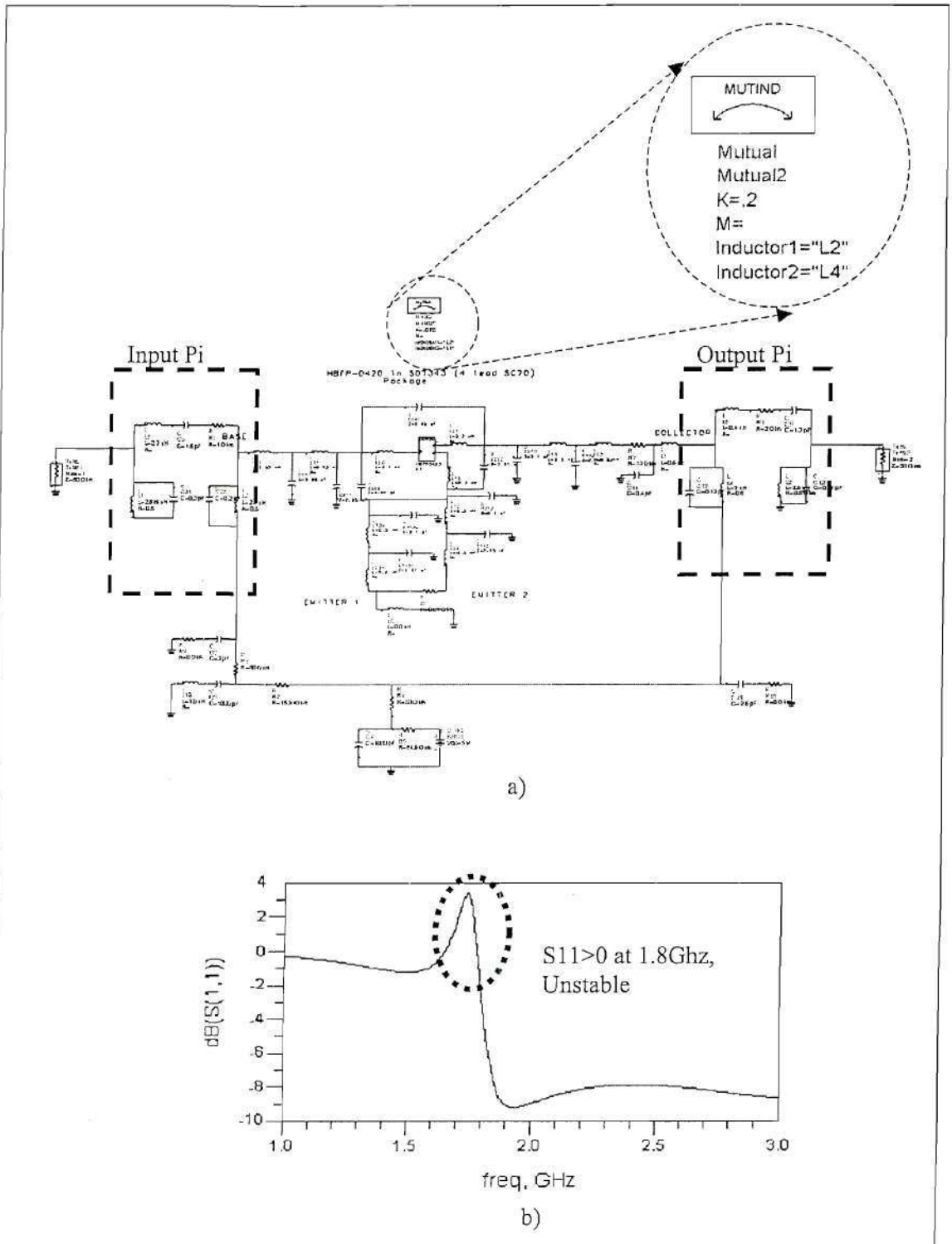


Fig 14 a) ADS circuit model for the LNA, along with the mutual inductance that was necessary to model the instability. **b)** Modeled (ADS) S11 results showing instability

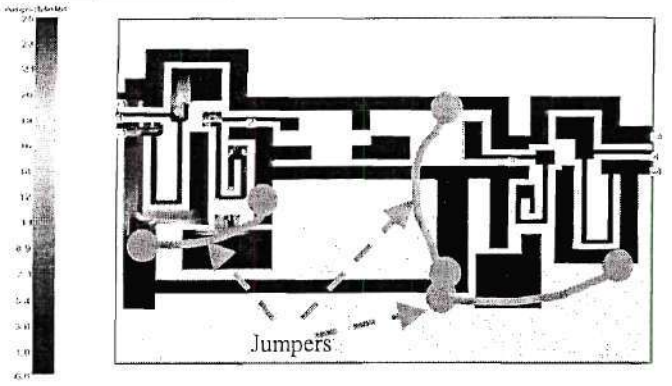


Fig 15. SONNET simulations of the unstable LNA layout, with the use of jumpers for current re-routing.

B) Modeling – Using Transmission Lines

Electromagnetic solvers take long computation times, and this further increases as the number of ports is increased. This makes it difficult to use tools like SONNET to model the mutual inductance in circuits at the design phase, when multiple simulations are required for optimizing the layout. For example, computing the coupling coefficient in the previous example at six frequencies using SONNET required twelve minutes of simulation time on a Sunblade 1000™ workstation. To reduce computation time, a circuit based modeling methodology was also used, based on transmission line theory [20].

Modeling each pi network as an equivalent circuit consisting of two inductors and one capacitor makes it difficult to model the effect of the reference ground layout. Non-idealities in the ground distribution were therefore analyzed by segmenting the structure into various coupled line sections [21]. Fig. 16 shows an example of the segmentation of two inductors (in CPW configuration) into several coupled line sections. Fig. 16b shows the layout of the inductors unfolded into a cascaded structure of coupled lines. Each

individual transmission line segment was defined by referencing it to the backside metallization of the packaging substrate. Fig 16c shows the cross-section of segment 4. The multilayer coupled line models (E.g. ML5CTL_V, ML1CTL_C etc.) in ADS were used to obtain the complete circuit model, with both signal and ground structures modeled as transmission line segments referenced to the backside metallization.

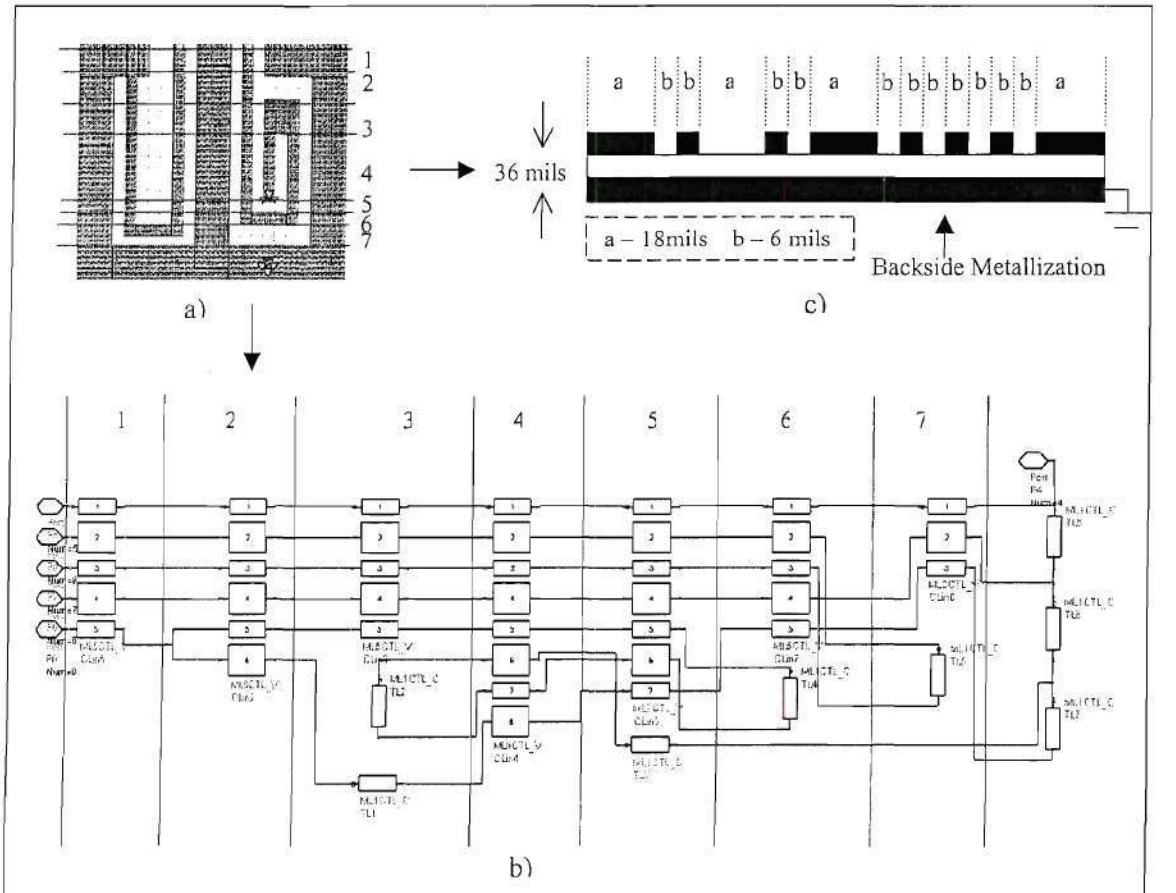


Fig 16. Coupled-line modeling of two inductors **a)** Layout and segmentation of the inductors **b)** ADS multilayer coupled line model of the inductors **c)** Cross-section of one of the segment (Segment 4)

Fig. 17 shows the modeled instability (in ADS). The circuit-based model was able to predict the frequency of instability, at the same time reducing the computation time by an order of magnitude (80 seconds) as compared to modeling using SONNET. It is to be

noted here that this modeling methodology is valid only at low frequencies (<5 Ghz). The accuracy of coupled-line modeling decreases as the ratio of the wavelength to the thickness of the dielectric decreases. The effect of discontinuities is also much higher at high frequencies. In addition, the model was successfully applied only for predicting the frequency of instability, and not its amplitude.

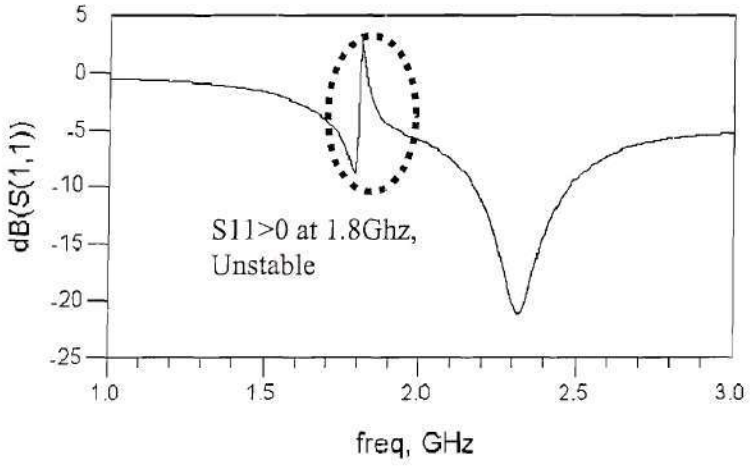


Fig. 17. Modeled (ADS) S11 results showing instability

VII. CONCLUSIONS

The use of high-Q passives embedded in the packaging substrate provides an opportunity for achieving complete system-level integration. Unlike discrete passives (with fixed Q's) and on-chip inductors (with very low Q's), the use of embedded inductors in the package (with a range of Q values from 20 to 170) results in the availability of a new design variable, namely the passive Q. However, higher inductor Q values come with the tradeoff of higher size. A novel optimization strategy incorporating the inductor Q and device size into the design methodology for integrated CMOS LNAs

has been developed. It has been shown that beyond a certain inductor Q, the NF becomes almost independent of Q. This optimum Q can therefore be used to determine the optimal size of the inductor, and thus reduce the packaged device size. This methodology can be applied for designing integrated CMOS LNAs using any of the common SOP technologies. Simulations show that a completely integrated device with a gain of 10 dB and a NF of 2.2 dB can be implemented using 0.5μ CMOS technology and an organic laminate based packaging substrate, with the packaged device measuring only 3.5 mm^2 in area.

A design and simulation methodology to integrate system level full-wave solvers into the design process for active devices with multiple embedded passives has been proposed and validated through measurement results. In addition, a computationally efficient circuit based modeling technique using coupled-line theory has also been developed, to predict the effect of coupling between multiple embedded passives in SOP based integration schemes. Hybrid LNAs using a combination of discrete and embedded components have been designed and fabricated, as test vehicles to study the effect of return current layout and coupling between multiple embedded passives on system performance. As shown in this paper, the layout of the reference ground and return current paths play a very important role in the performance of the LNA.

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Automation Systems) for assistance during the assembly of the devices. In addition, they are indebted to Sung-Hwan Min for the many helpful discussions throughout the duration of this project. Finally, they would like to thank National Science Foundation (NSF) and Semiconductor Research Corporation (SRC), who supported this work under grants DMI-0120308 and 2001-NJ-940 respectively.

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